

Do silício ao carbono: novos rumos para o transporte eletrônico?



Caio Lewenkopf - UFF

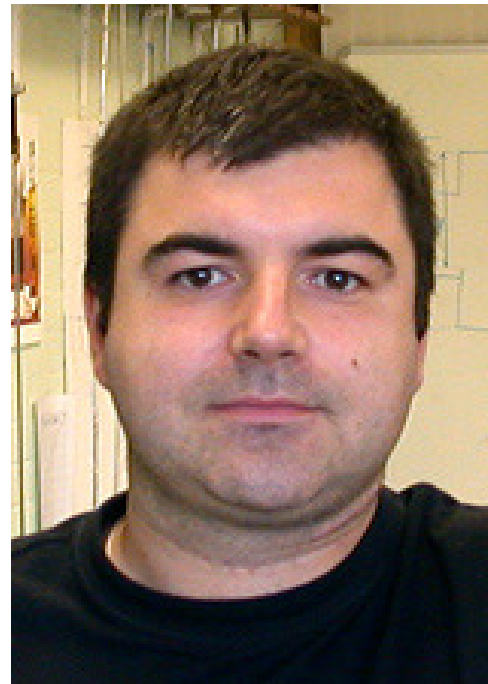


Prêmio Nobel de Física - 2010

"por experimentos pioneiros relacionados ao material bidimensional grafeno"



Andre Geim



Konstantin Novoselov

Nem sempre foi assim...



Eur. J. Phys. 18 (1997) 307–313. Printed in the UK

PII: S0143-0807(97)84689-2

Of flying frogs and levitrons

M V Berry[†] and A K Geim[‡]

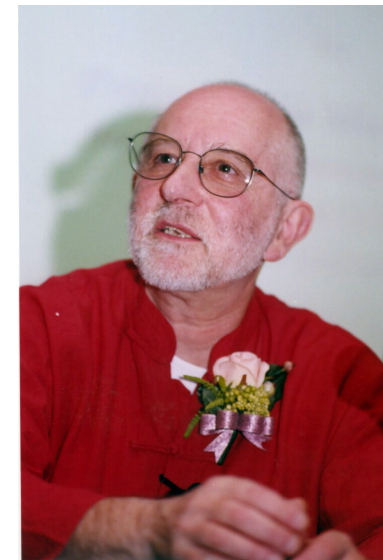
[†] H H Wills Physics Laboratory, Tyndall Avenue, Bristol BS8 1TL, UK

[‡] High Field Magnet Laboratory, Department of Physics, University of Nijmegen, Toernooiveld, 6525 ED Nijmegen, The Netherlands

Prêmio Ignobel

Física 2000

A. Geim e M. Berry



Nem sempre foi assim...



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Of flying frogs and levitrons

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Microfabricated adhesive mimicking gecko foot-hair

A. K. Geim, K. S. Novoselov e outros

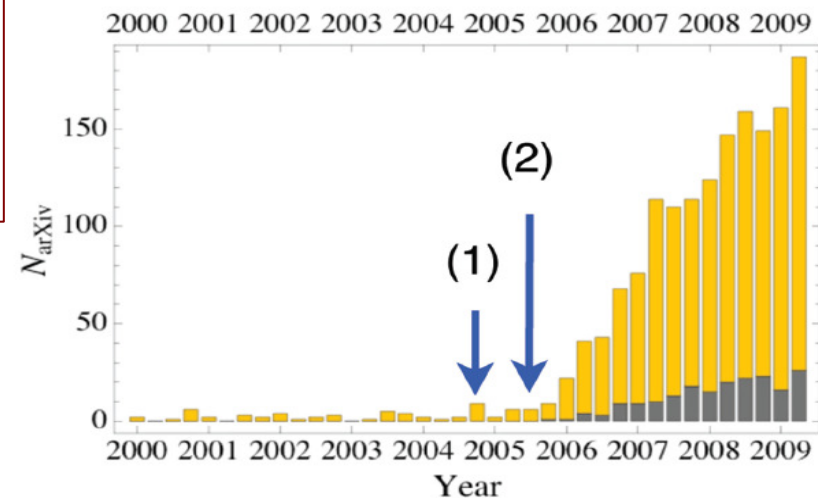
Nature Materials **2**, 461 - 463 (2003)

Nascimento de um campo de pesquisa

Science 306, 666 (2004)

Electric Field Effect in Atomically Thin Carbon Films

K. S. Novoselov,¹ A. K. Geim,^{1*} S. V. Morozov,² D. Jiang,¹
Y. Zhang,¹ S. V. Dubonos,² I. V. Grigorieva,¹ A. A. Firsov²

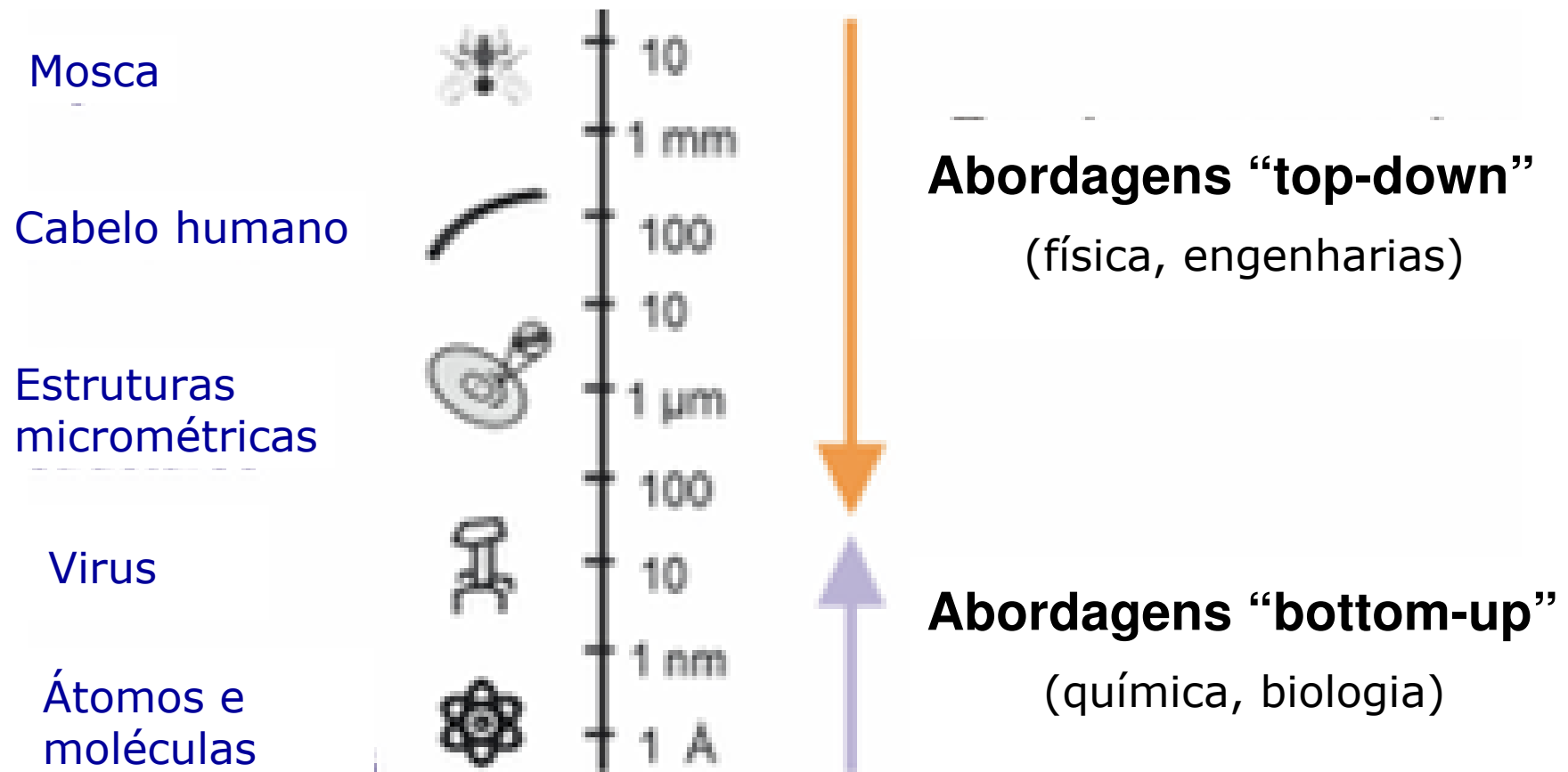


Vol 438|10 November 2005|doi:10.1038/nature04233

Two-dimensional gas of massless Dirac fermions in graphene

K. S. Novoselov¹, A. K. Geim¹, S. V. Morozov², D. Jiang¹, M. I. Katsnelson³, I. V. Grigorieva¹, S. V. Dubonos²
& A. A. Firsov²

O que nanotecnologia?



De onde surgiu a idéia?



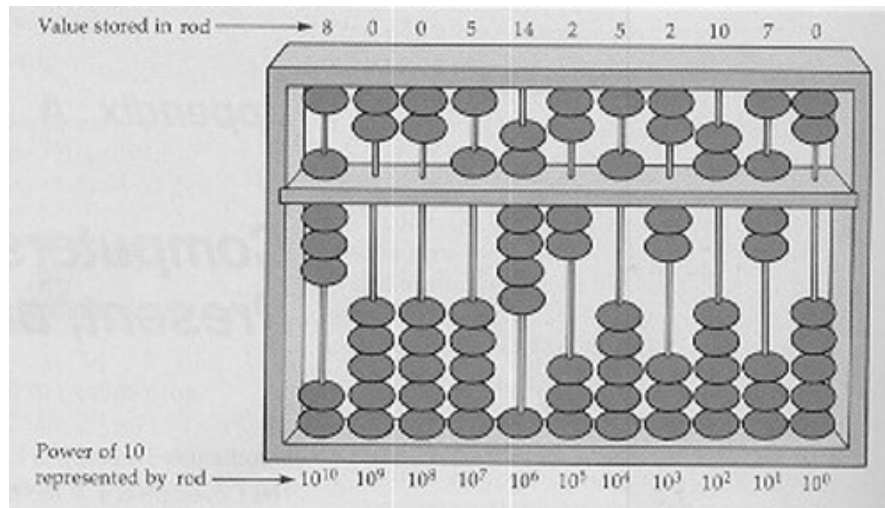
Richard P. Feynman

palestra na Caltech, EUA (1959)

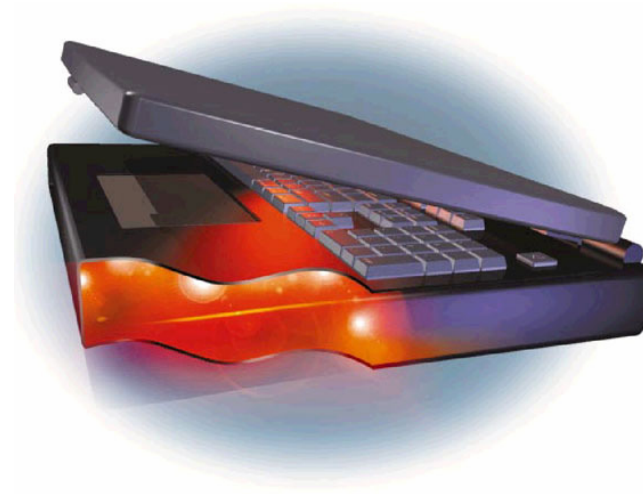
"Há muito espaço embaixo"

- Por que não podemos transcrever toda Enciclopédia Britânica na cabeça de um alfinete?
- Por que não podemos reduzir o tamanho de motores elétricos para escalas de comprimento moleculares?

Física e a revolução na informação



ábaco – 500 A.C. – 10 adições / min

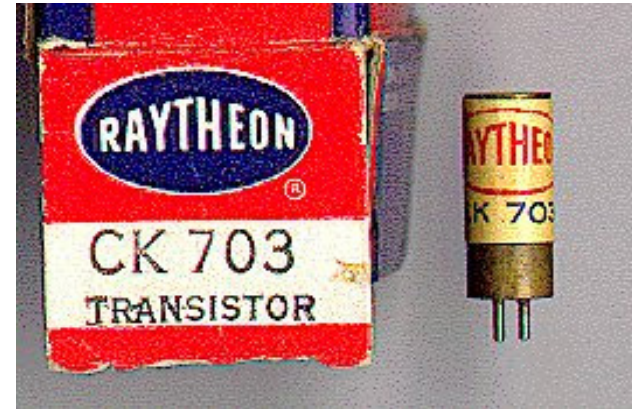


Intel Core i5 – 2010 D.C. – 10^9 adições / s

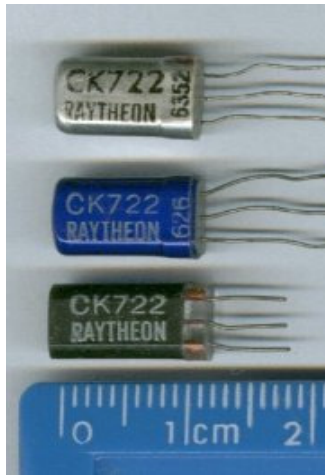
Evolução dos transistores



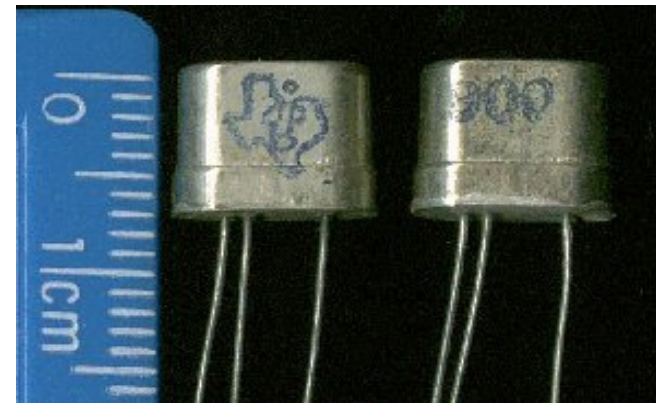
1948- Schockly
inventa o transistor de junção de Ge



1949- Raytheon CK703
Primeiro transistor comercial de Ge



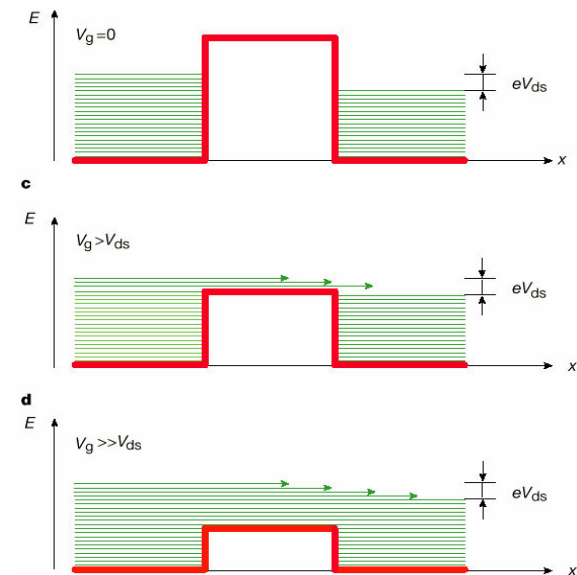
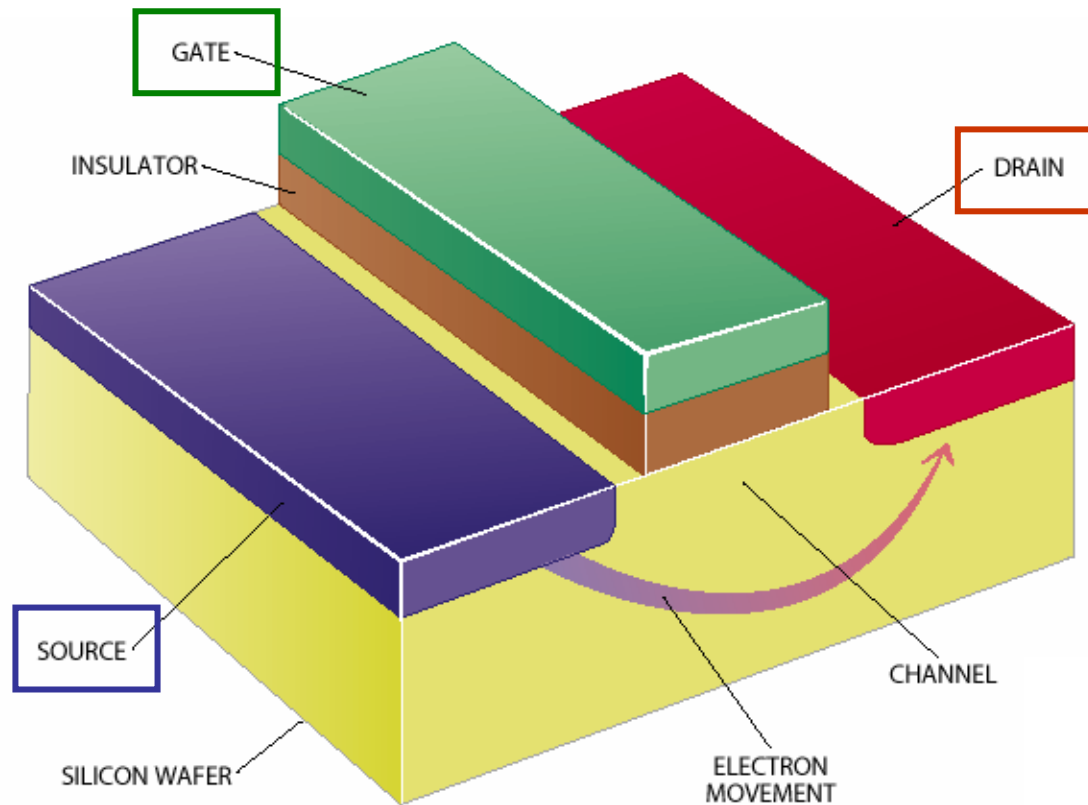
1953 - Raytheon CK722
Primeiro transistor de Ge produzido em massa



1955 - Texas Instruments 900
Primeiro transistor comercial de Si

Transistor como amplificador & chave

Transistor de efeito de campo (FET)



pequena voltagem de *porta* controla uma grande corrente de *dreno*

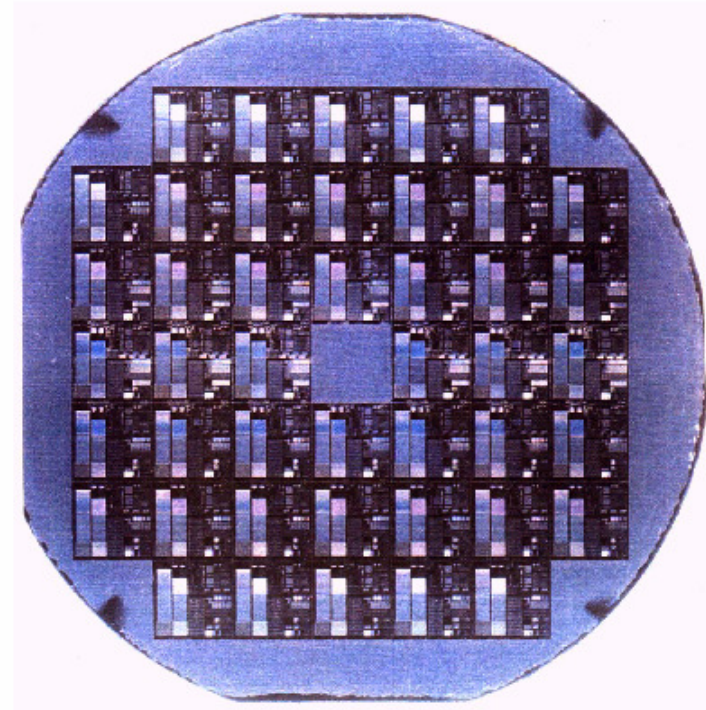
inventando o *circuito integrado*

- muitos transistores e circuitos complexos em um **único** substrato -



Primeiro circuito integrado produzido
pela
Texas Instruments

1958 - Jack Kilby e Robert Noyce



circuito integrado moderno
cada chip contem muitos milhões de
transistores



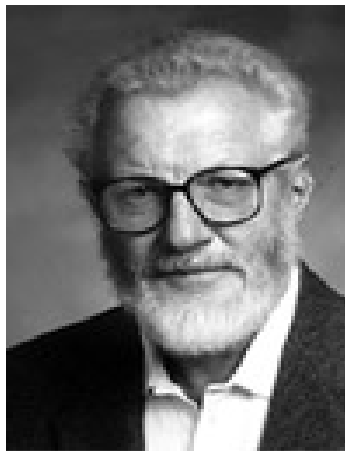
Prêmio Nobel de Física - 2000

"pelo trabalho fundamental em informação e tecnologia de comunicação"

"pelo desenvolvimento de heteroestruturas semicondutoras usadas em aplicações de alta velocidade e opto-eletrônica"

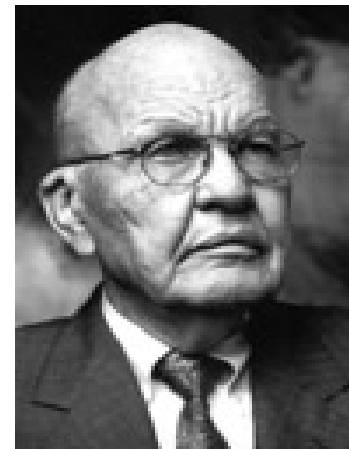


Zhores I Alferov



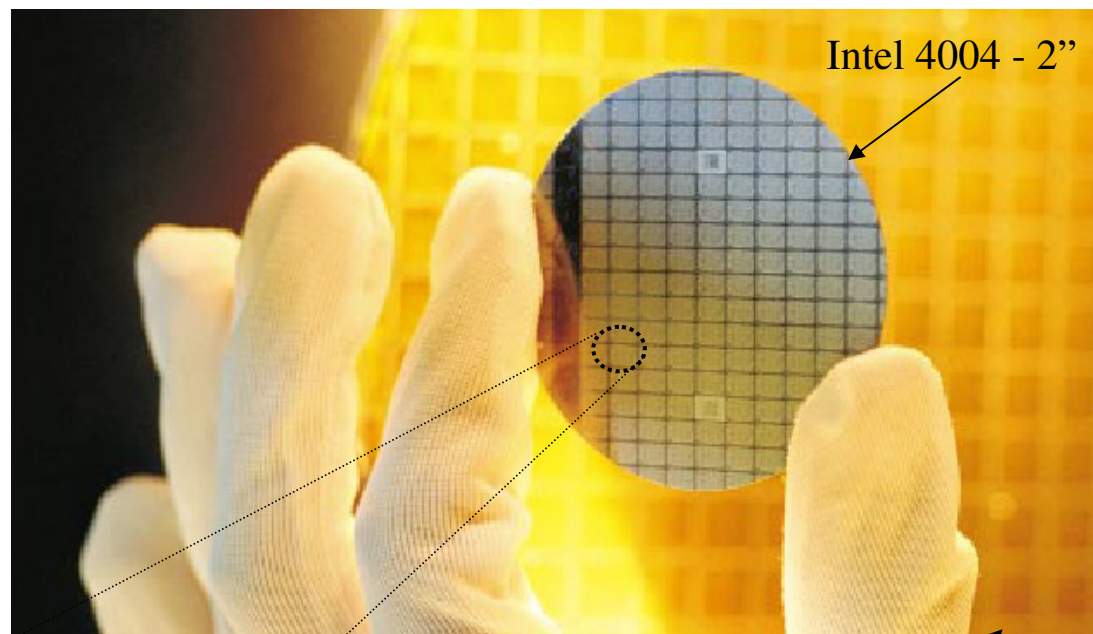
Herbert Kroemer

"pela sua atuação na invenção do circuito integrado"

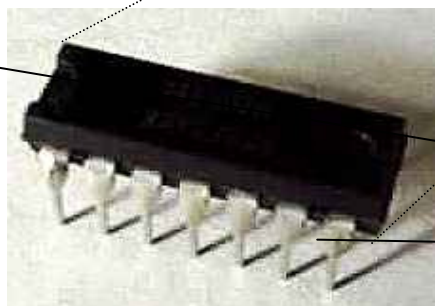


Jack S Kilby

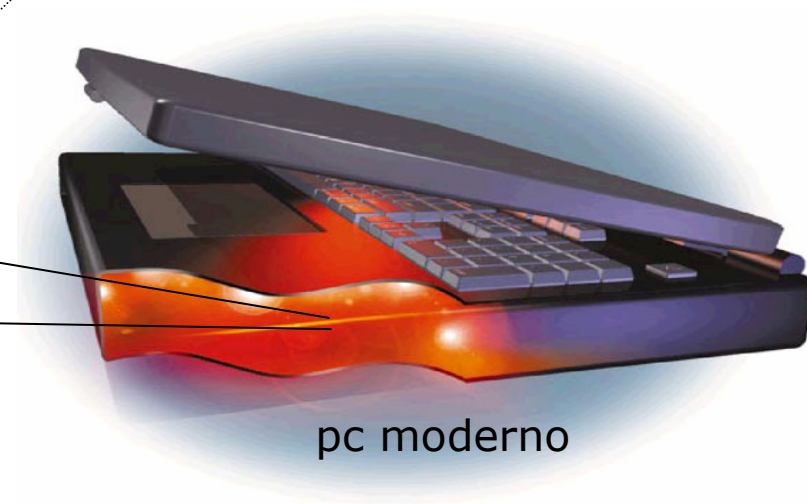
circuitos integrados coração do computador



wafers hoje-12"



chip



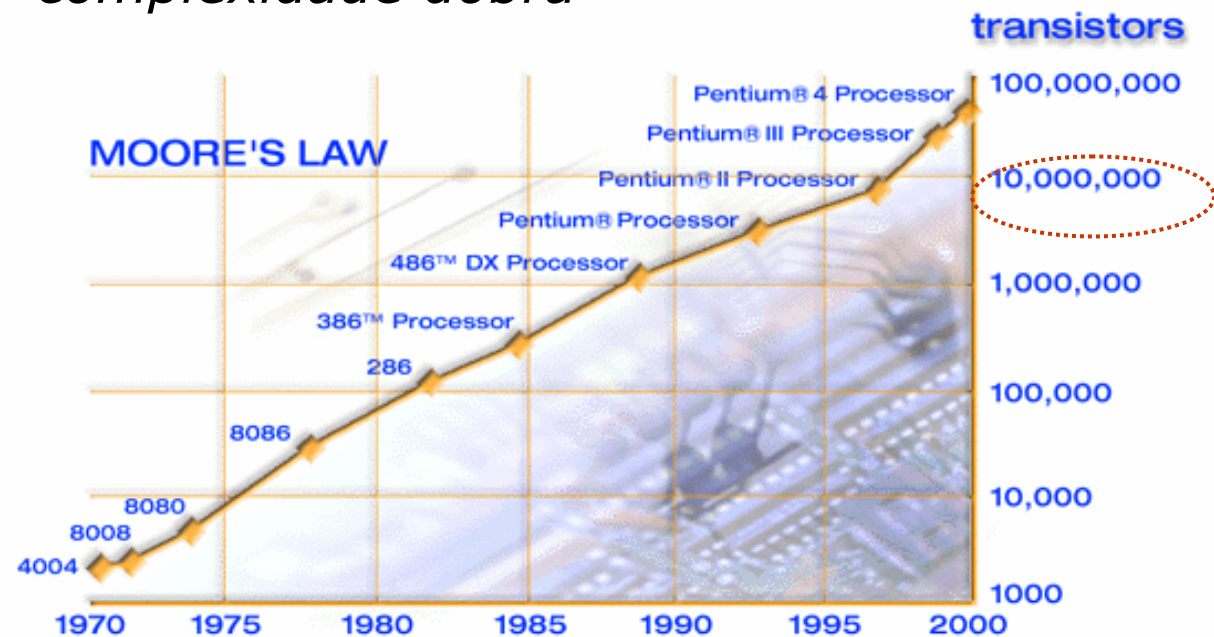
pc moderno

Lei de Moore

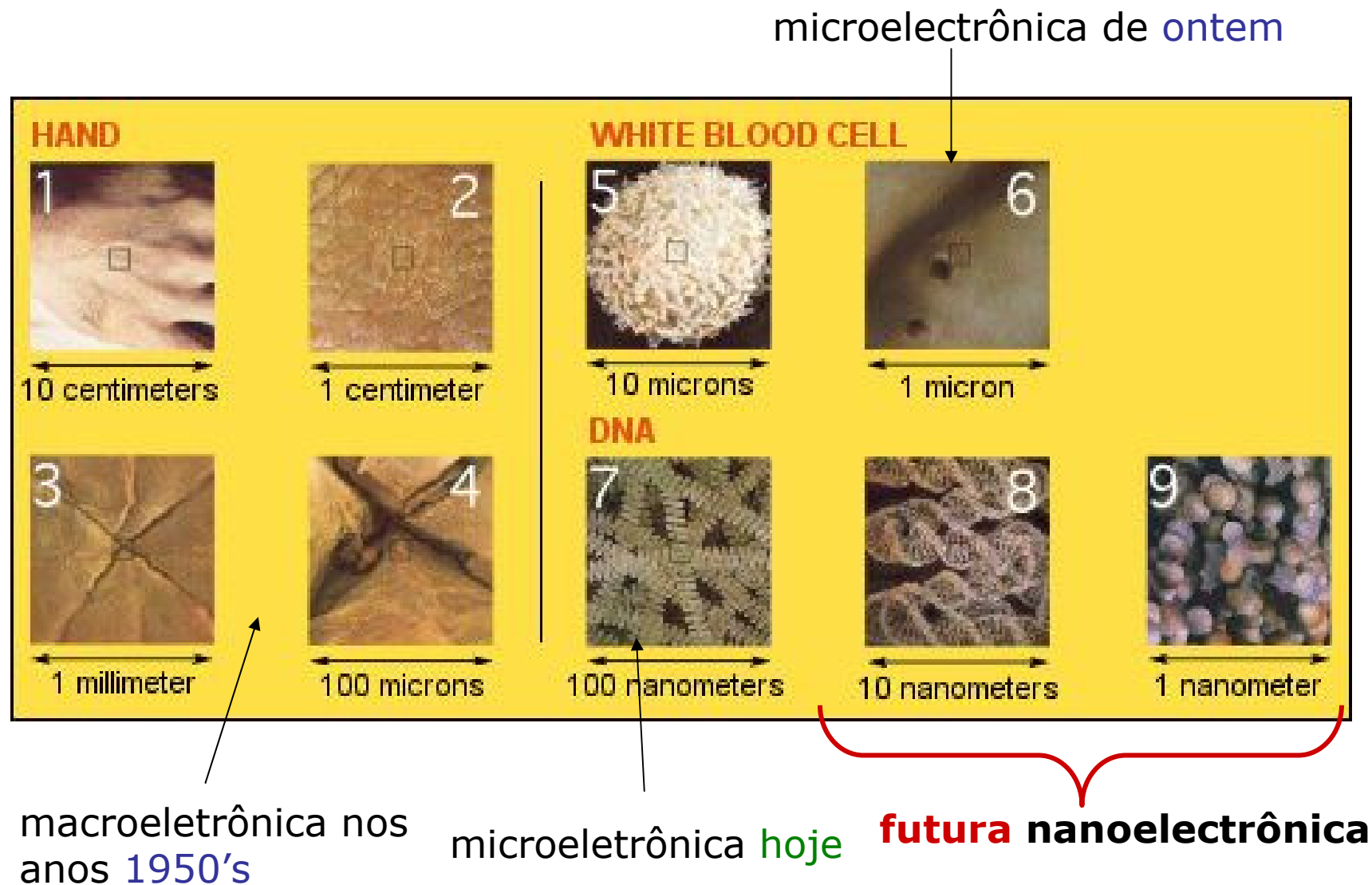


Gordon Moore

"a cada 1,5 anos a complexidade dobra"



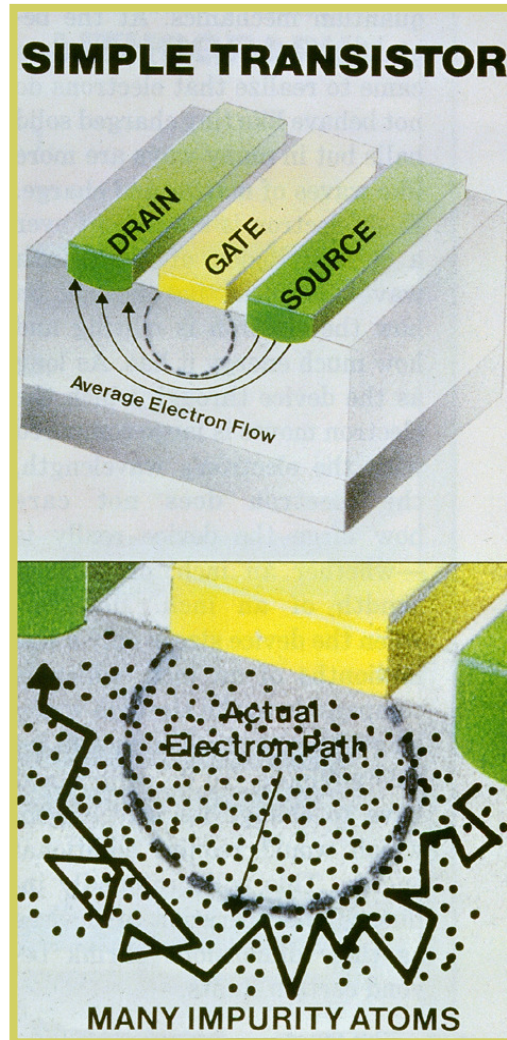
Continuando o processo de "scale down"



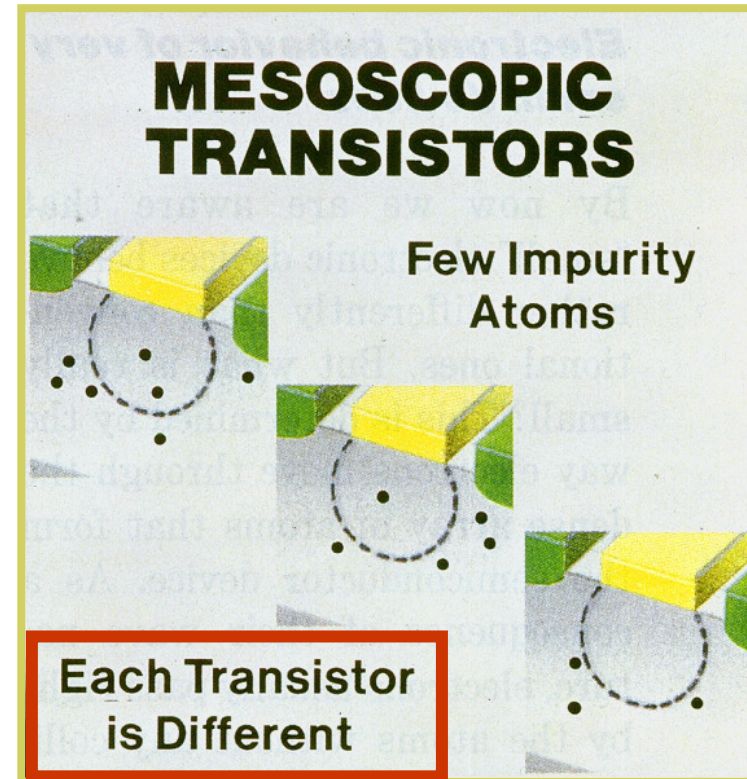
Quais as novidades conceituais da nanoeletrônica ?

Um problema imediato: simples estatística

hoje



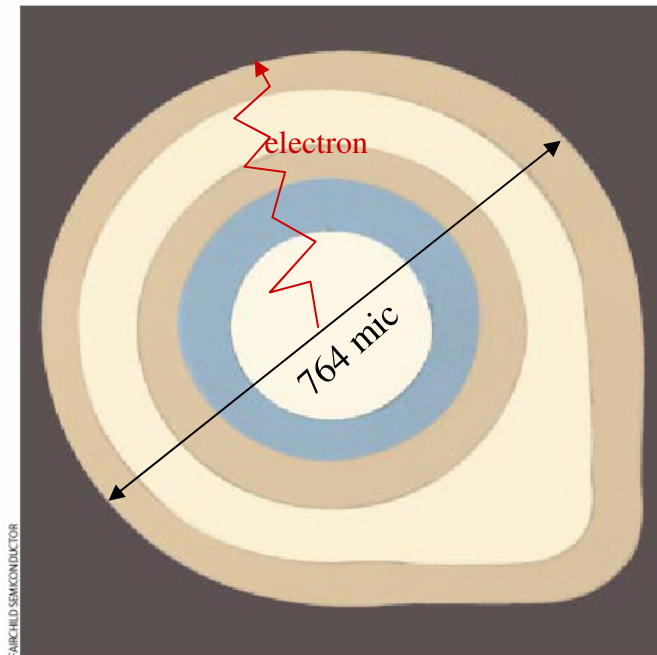
futuro



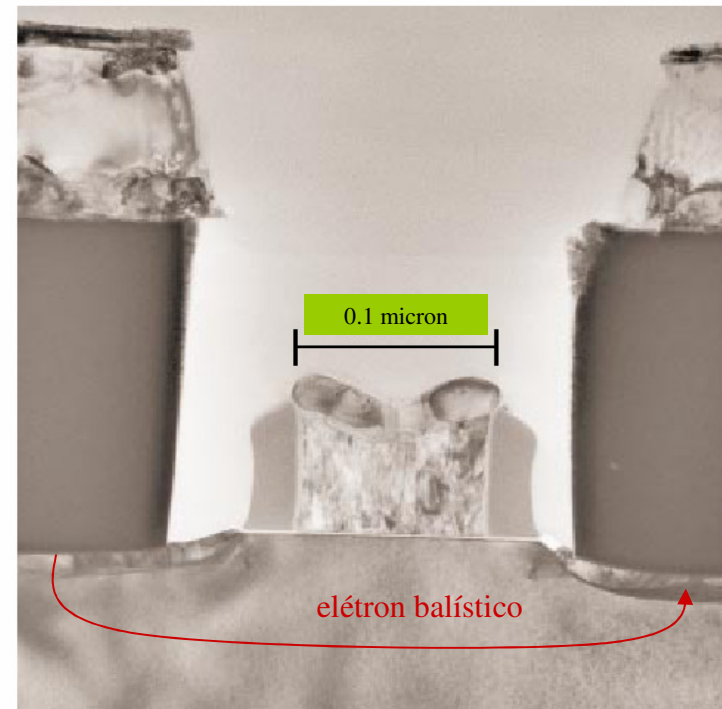
todos transistores são similares
por causa de *self averaging*

De muitas impurezas ... para muito poucas

Fairchild - 1959

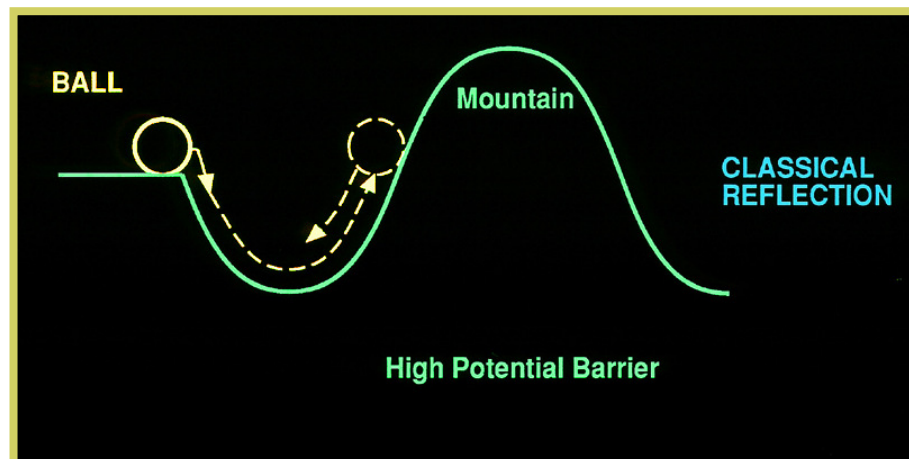


Intel - 2004

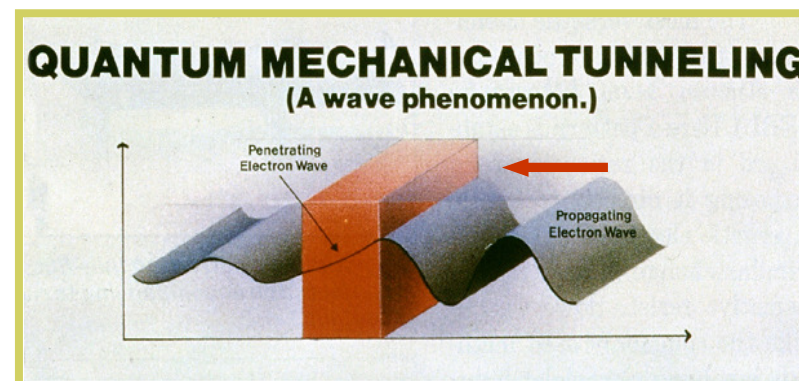


elétrons movendo-se sem colisões

Uma das maravilhas da mecânica quântica: Efeito túnel



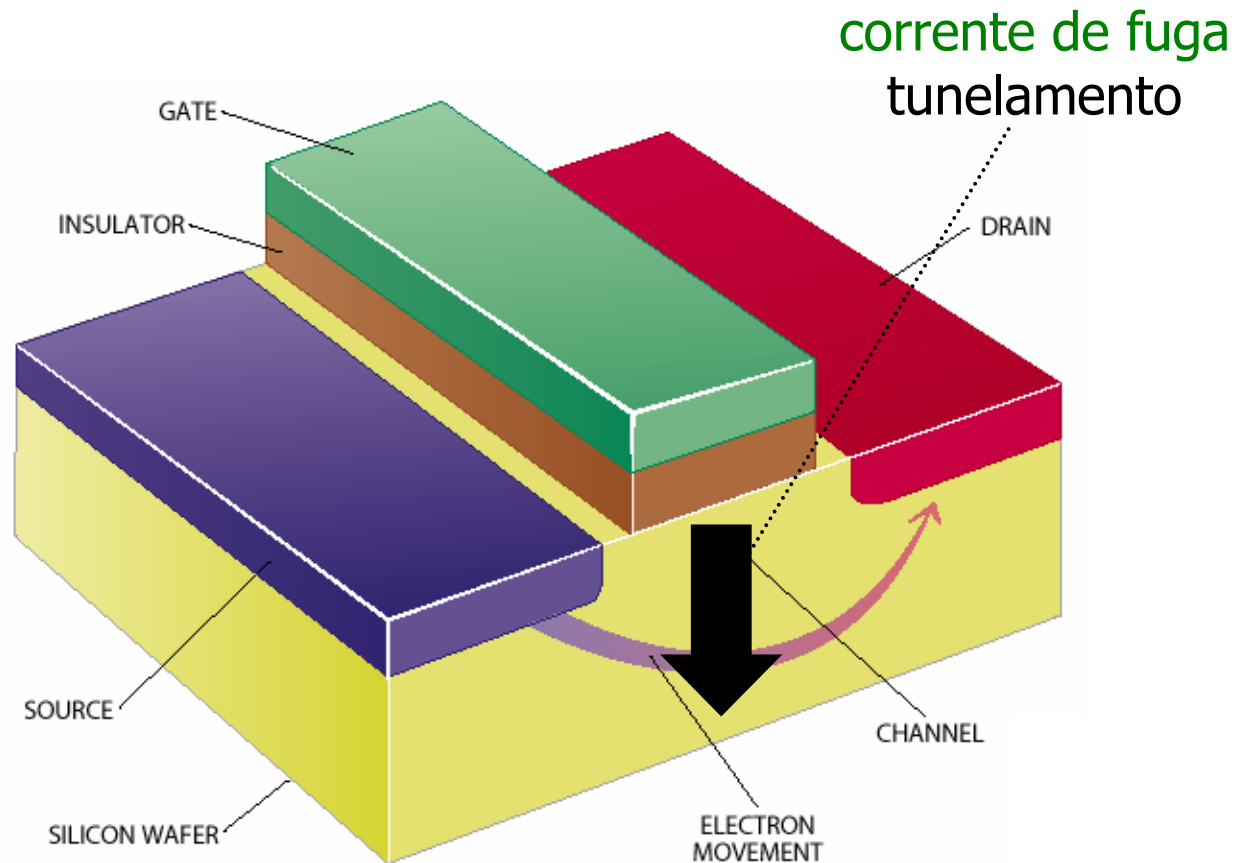
natureza ondulatória
dos elétrons



Tunelamento: consequências

**pequenas correntes fluem
através
de circuitos ABERTOS**

tunelamento: limite para a miniaturização de dispositivos





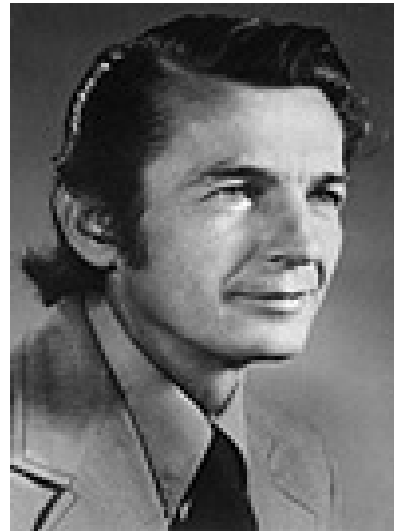
Prêmio Nobel de Física - 1973

"por suas descobertas experimentais de fenômenos de tunelamento em semi-condutores e em super-condutores respectivamente"

"por sua predição teórica das propriedades de uma supercorrente através de uma barreira de tunelamento, em particular dos fenômenos que são geralmente conhecidos como efeitos Josephson"



Leo Esaki

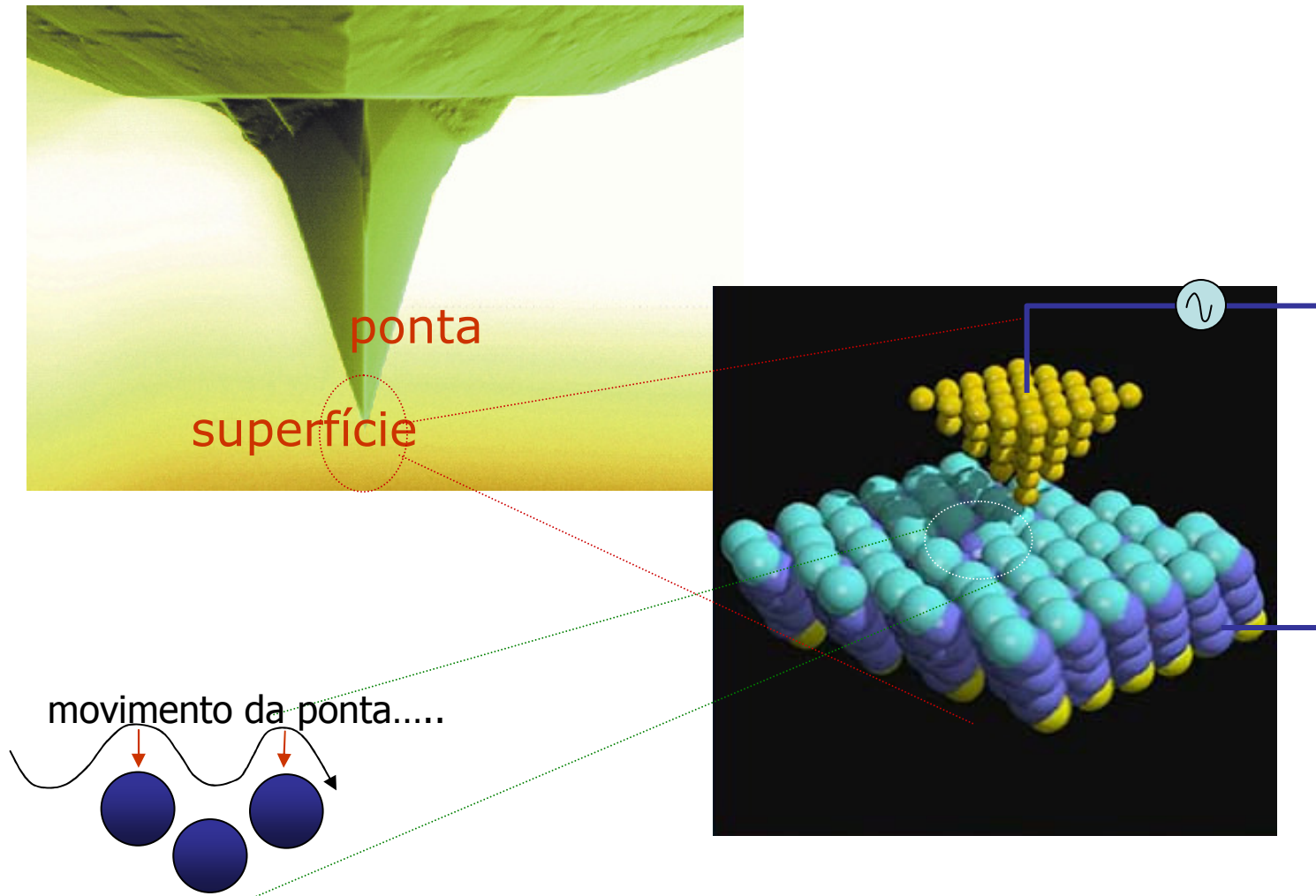


Ivar Giaever



Brian Josephson

Revolução do tunelamento: Scanning Tunneling Microscope





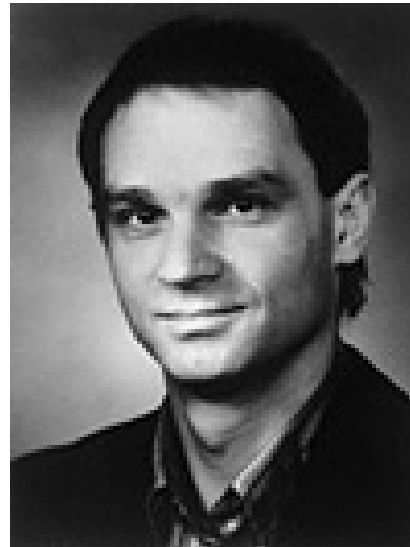
Prêmio Nobel de Física - 1986

“por seu trabalho fundamental em ótica eletrônica e pelo desenho do primeiro microscópio eletrônico”

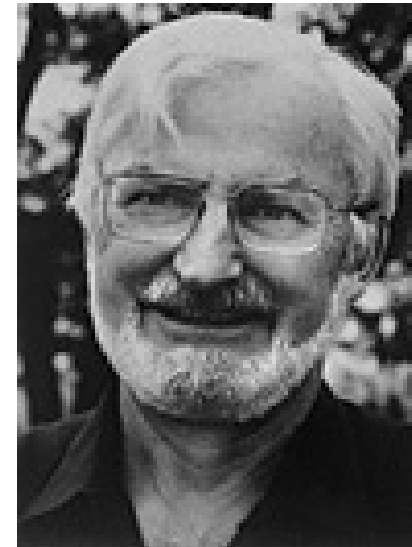


Ernst Ruska

“pelo seu desenho do microscópio de tunelamento de varredura”



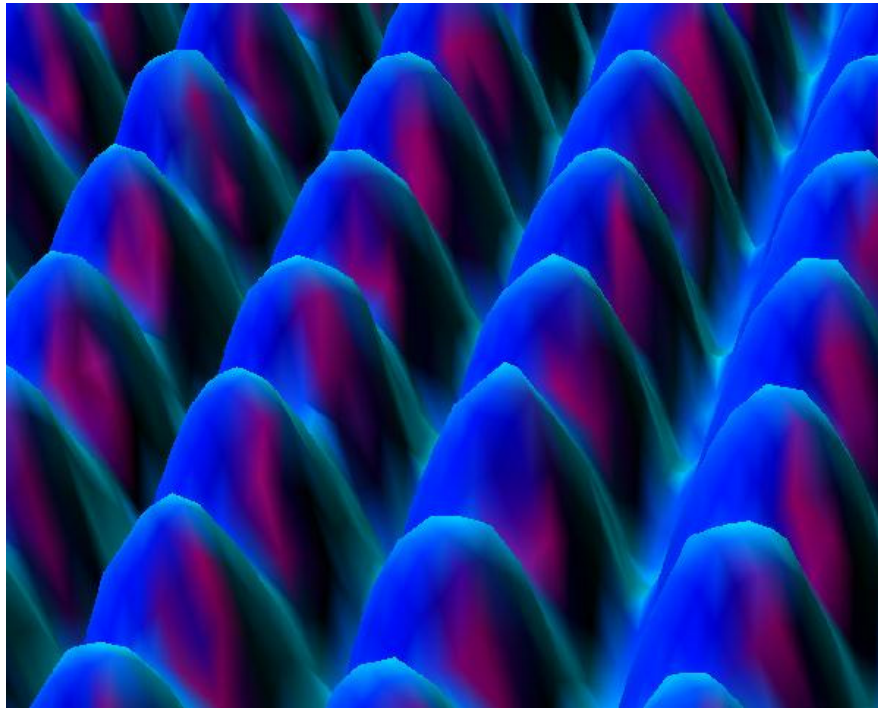
Gerd Binnig



Heinrich Rohrer

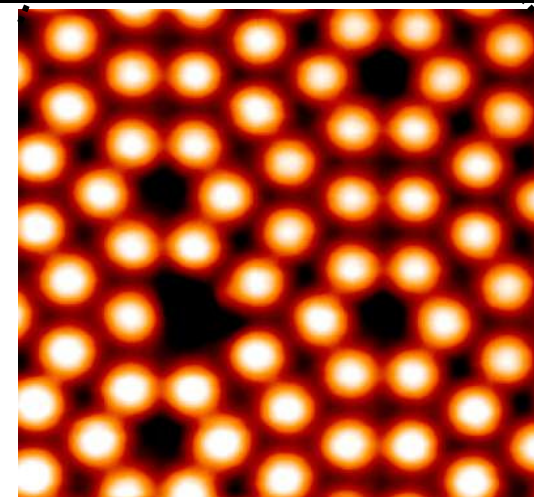
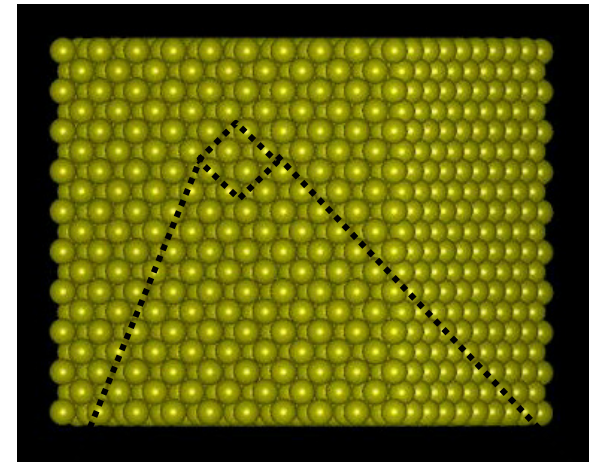
STM observando superfícies

níquel

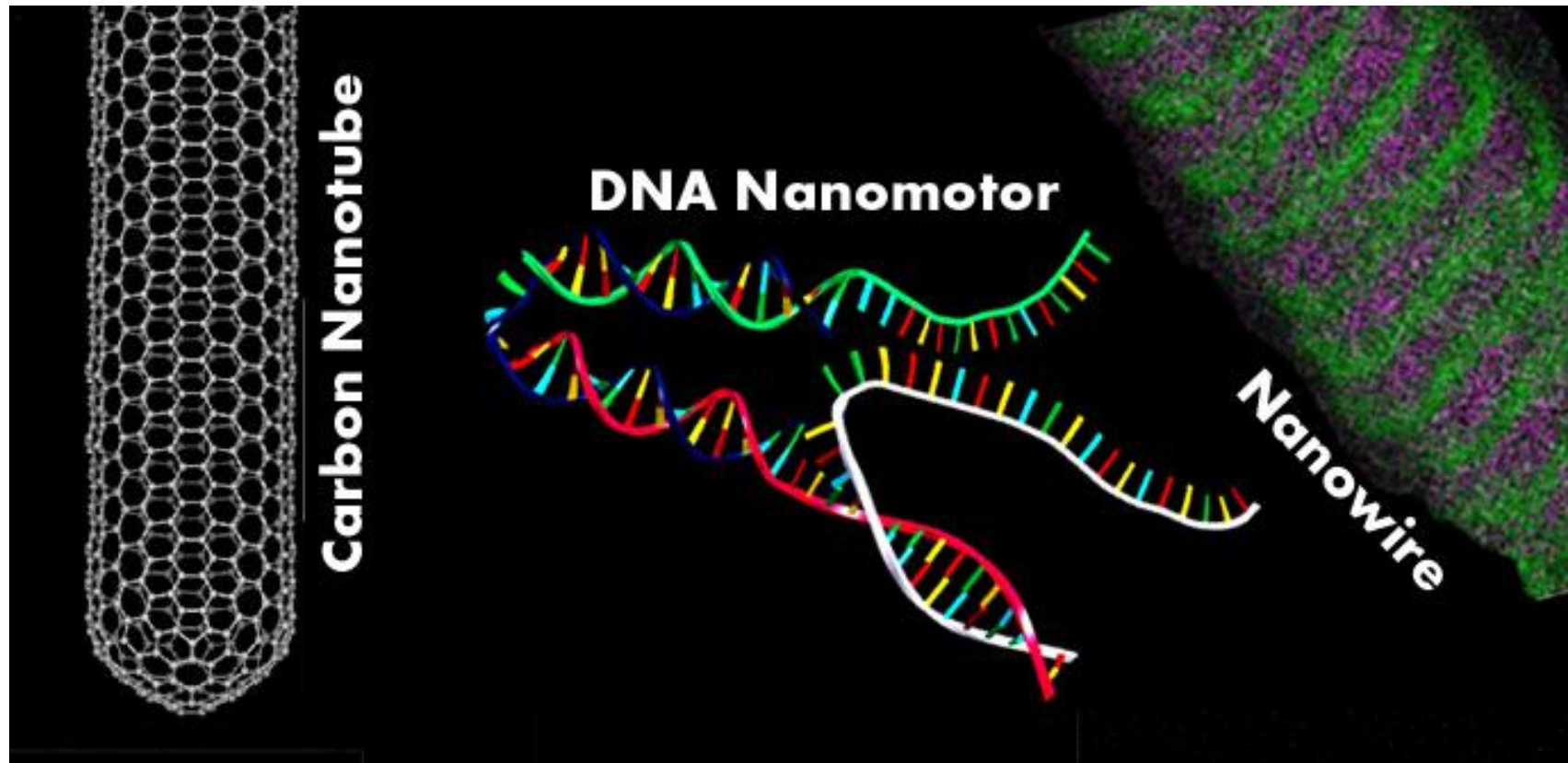


←→
3 Angstroms = 0.3 nm

silício



Bottom-up: começando pelos constituintes básicos



Eletrônica molecular – outra palestra

Estruturas com nanotubos

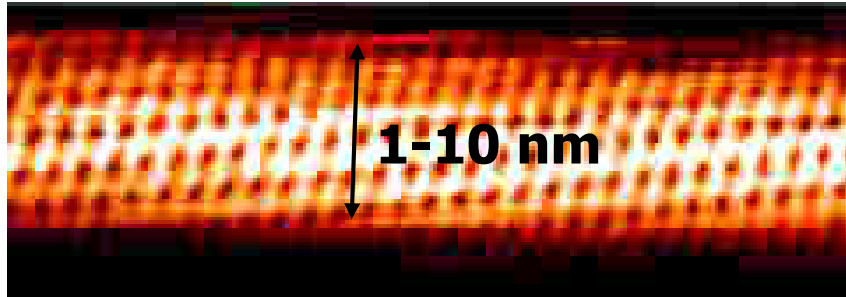
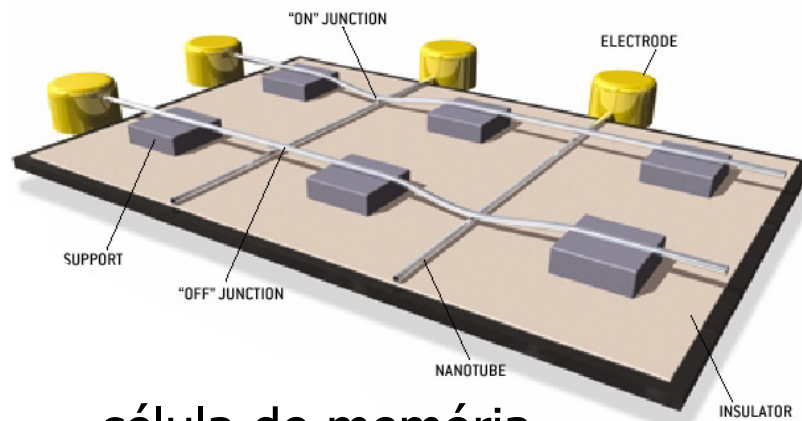
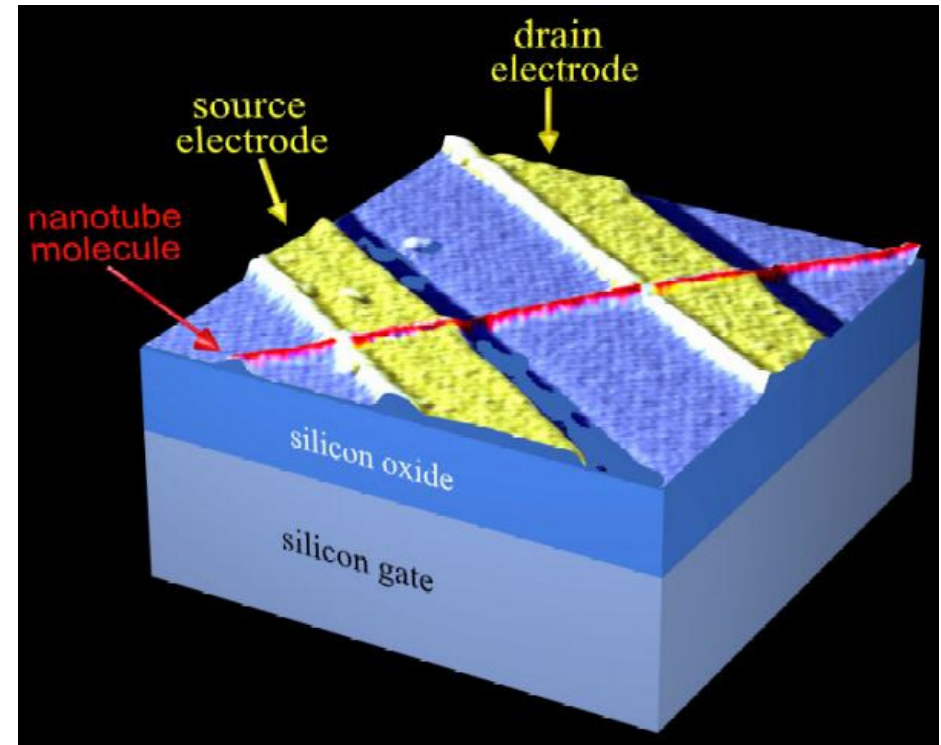


imagem de nanotubo

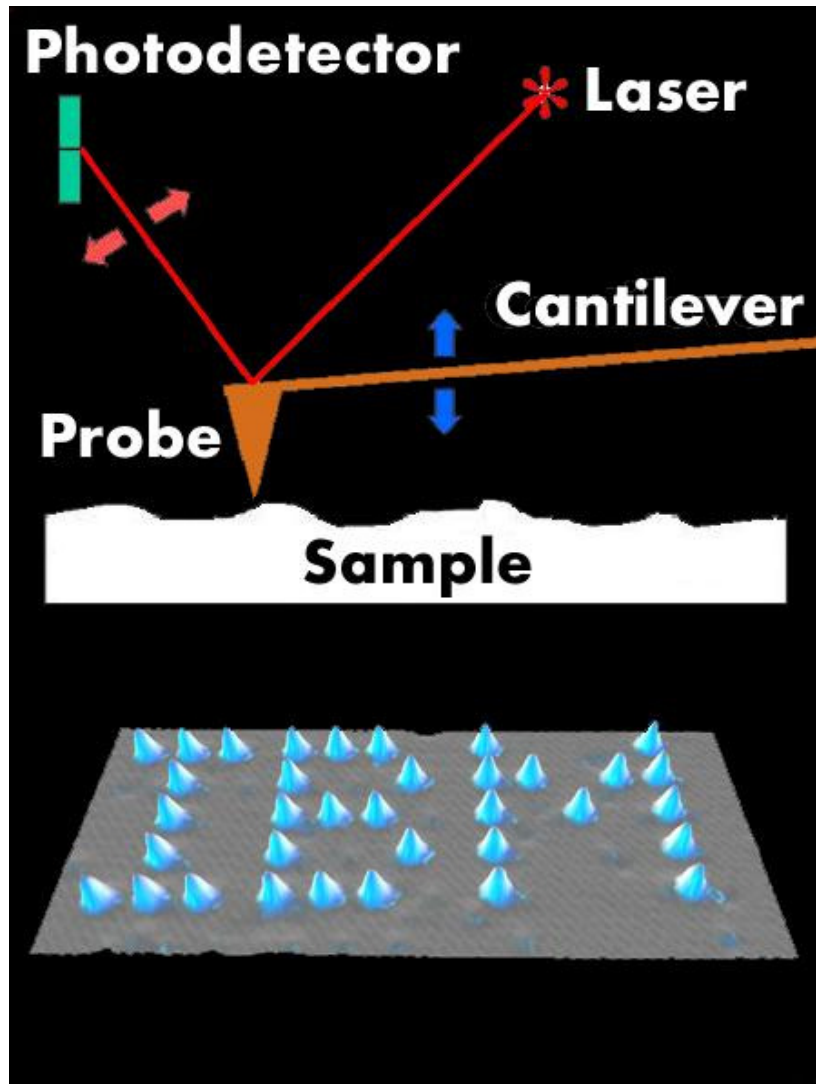


célula de memória

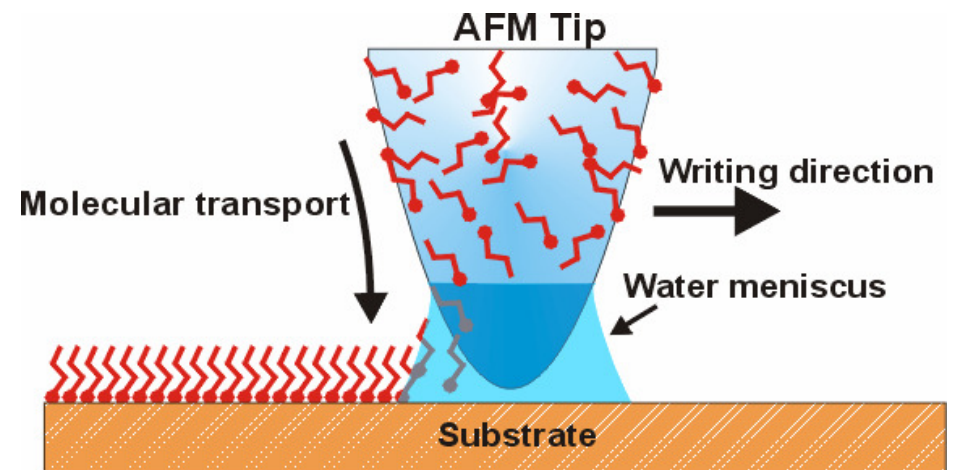


transistor unidimensional

Pegar e colar

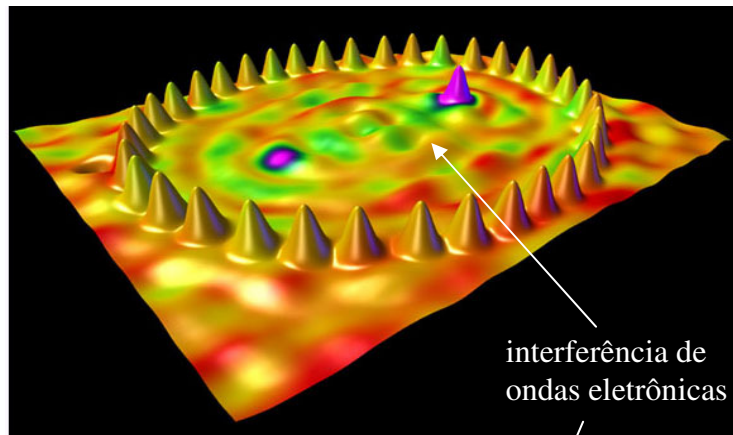


escrever



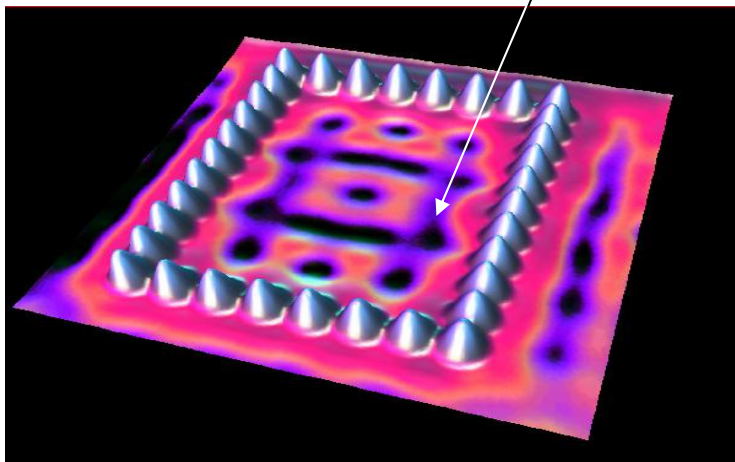
ponta AFM (como STM)

Pegar e colar

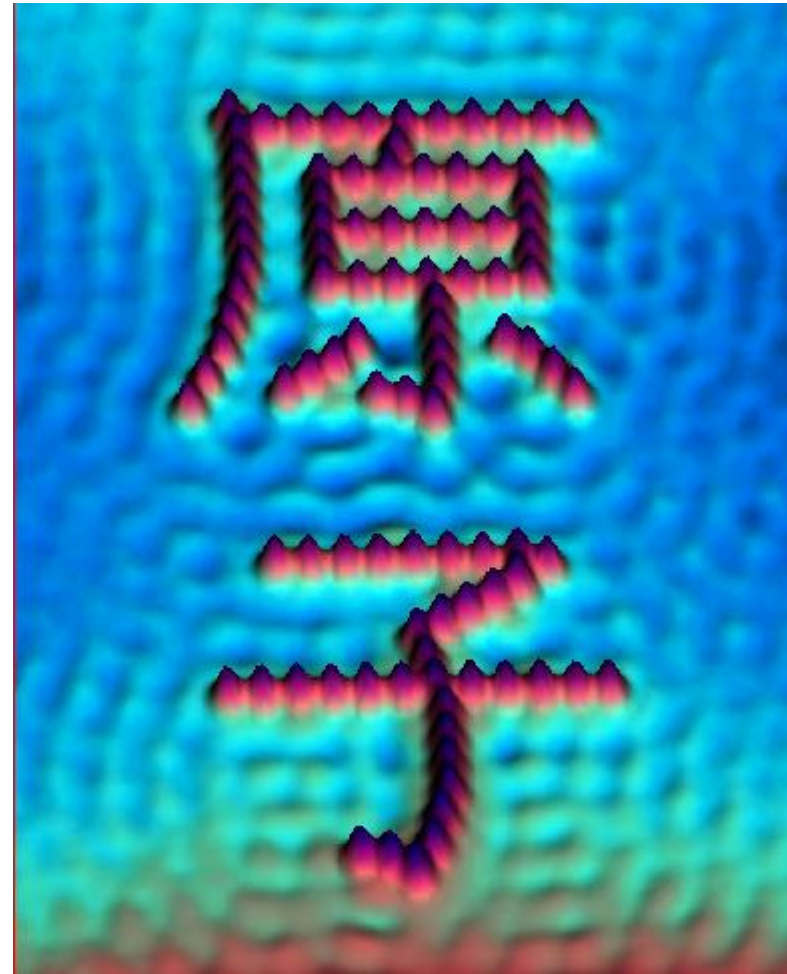


interferência de
ondas eletrônicas

estádio circular



estádio quadrado



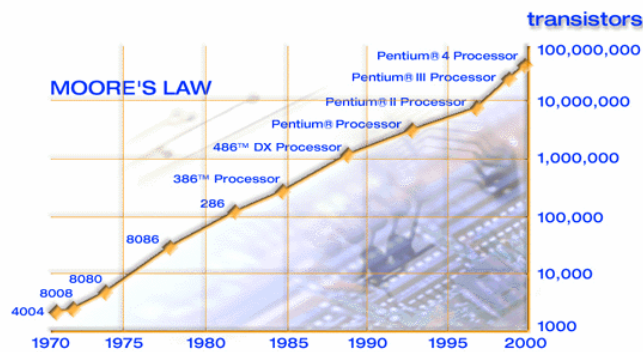
Kanji para *ÁTOMO*

Lei de Moore e o Silício

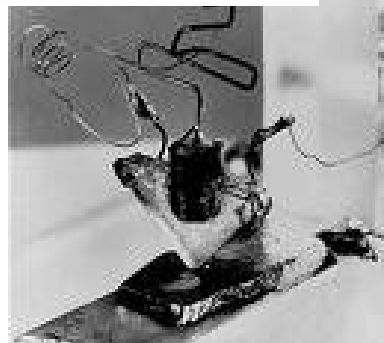
- Dissipação de calor.
 - No momento, micro-processadores de 500 MHz com 10 milhões de transistores emitem quase 100W
- Vazamento de um dispositivo para o outro
 - A estrutura de bandas do silício possibilita uma grande variedade de energias para os electrons. Alguns eletrons podem ganhar energia suficiente para tunelar de um dispositivo para outro
- Acoplamento capacitivo entre os dispositivos.
- Métodos de fabricação (fotolitografia).
 - O tamanho do dispositivo é limitado pela difração – aproximadamente meio comprimento de onda da luz utilizada no processo de litografia.
- 'Silicon Wall'
 - Para comprimentos de 50 nm ou menores não é possível dopar o silício uniformemente (isto é o fim da linha para o comportamento tipo bulk).

Mapa tecnológico de semicondutores

Por que não pensar em materiais que não o Si?



1947
William Shockley
John Bardeen
Walter Brattain



B 5 10.81 Boron	C 6 12.01 Carbon	N 7 14.01 Nitrogen
Al 13 26.98 Aluminum	Si 14 28.09 Silicon	P 15 30.97 Phosphorus
Ga 31 69.72 Gallium	Ge 32 72.61 Germanium	As 33 74.92 Arsenic
In 49 75.37 Indium	Sn 50 118.71 Tin	Sb 51 121.75 Antimony

Carbono e eletrônica: por que é interessante?

Where we stand in the push for miniaturization and higher speeds :

Materials technology metrics*

2012

Table FEP2

Starting Materials Technology Requirements—Near and Long-term Years

Year of Production	2007	2008	2009	2010	2011	2012
DRAM % Pitch (nm) (contacted)	68	58	52	45	40	36
MPU/ASIC Metal 1 (M1) % Pitch (nm)(contacted)	68	58	52	45	40	36
MPU Physical Gate Length (nm)	42	28	27	24	22	20
DRAM Total Chip Area (mm ²)	107	81	81	93	74	59
DRAM Active Transistor Area (mm ²)	23.4	29.3	19.2	29.1	23.1	18.3
MPU High-Performance Total Chip Area (mm ²)	310	246	195	310	246	195
MPU High-Performance Active Transistor Area (mm ²)	31.7	25.1	20.0	31.7	25.1	20.0
General Characteristics * (99% Chip Yield)						
Maximum Substrate Diameter (mm)—High-volume Production (>30k-wafer-starts-per-month)	300	300	300	300	300	450
Edge exclusion (mm)	2	2	2	2	2	2
Front surface particle size (mm), latex sphere equivalent (A)	≤65	≤65	≤65	≤65	≤65	≤45
Particles (cm ⁻²)	≤0.33	≤0.33	≤0.32	≤0.15	≤0.15	≤0.32
Particles (#/wt)	≤238	≤238	≤215	≤105	≤105	≤496
Site flatness (mm), 5FQR 26mm x 8 mm Site Size	≤68	≤59	≤52	≤45	≤40	≤36
Nanotopography: p-v, 2 mm dia. analysis area (I)	≤17	≤15	≤13	≤11	≤10	≤9
Epitaxial Wafer * (99% Chip Yield)						
Large structural epi defects (DRAM) (cm ⁻²) (B)	≤0.009	≤0.012	≤0.016	≤0.011	≤0.014	≤0.017
Large structural epi defects (MPU) (cm ⁻²) (B)	≤0.003	≤0.004	≤0.005	≤0.003	≤0.004	≤0.005
Small structural epi defects (DRAM) (cm ⁻²) (C)	≤0.019	≤0.025	≤0.033	≤0.022	≤0.027	≤0.034
Small structural epi defects (MPU) (cm ⁻²) (C)	≤0.006	≤0.008	≤0.010	≤0.006	≤0.008	≤0.010
Silicon-On-Insulator Wafer * (99% Chip Yield)						
Edge exclusion (mm)	2	2	2	2	2	2
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (mm) (D)	58-100	54-93	50-76	46-71	43-65	40-60
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3σ) (mm) (E)				16-31	16-20	15-19
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3σ) (mm) (F)				36-60	34-56	30-50
D _{1,AREA} Large area SOI wafer defects (DRAM) (cm ⁻²) (G)	≤0.009	≤0.012	≤0.016	≤0.011	≤0.014	≤0.017
D _{1,AREA} Large area SOI wafer defects (MPU) (cm ⁻²) (G)	≤0.003	≤0.004	≤0.005	≤0.003	≤0.004	≤0.005
D _{1,AREA} Small area SOI wafer defects (DRAM) (cm ⁻²) (H)	≤0.150	≤0.198	≤0.262	≤0.175	≤0.218	≤0.274
D _{1,AREA} Small area SOI wafer defects (MPU) (cm ⁻²) (H)	≤0.159	≤0.200	≤0.252	≤0.159	≤0.200	≤0.252

manufacturable solutions exist

manufacturable solutions known

manufacturable solutions unknown

* International Technology Roadmap for Semiconductors - 2008 Revision (<http://www.itrs.net/>)

Panorama da Física

10/2010

Carbono e eletrônica: por que é interessante?

Where we stand in the push for miniaturization and higher speeds :

Materials technology metrics*

2012 2020

Table FEP2 Starting Materials Technology Requirements—Near and Long-term Years

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
DRAM % Pitch (nm) (contacted)	58	58	52	45	40	36	32	28	25	23	20	18	16	14
MPU/ASIC Metal 1 (M1) % Pitch (nm)(contacted)	68	58	52	45	40	36	32	28	25	23	20	18	16	14
MPU Physical Gate Length (nm)	102	78	72	63	55	48	42	37	33	30	27	24	21	19
DRAM Total Chip Area (mm ²)	107	81	61	53	44	38	33	29	26	23	20	18	16	14
DRAM Active Transistor Area (mm ²)	11.7	7.8	5.9	5.1	4.3	3.7	3.2	2.8	2.5	2.3	2.0	1.8	1.6	1.4
MPU High-Performance Total Chip Area (mm ²)	310	246	195	168	145	126	110	97	86	77	68	60	53	46
MPU High-Performance Active Transistor Area (mm ²)	31.7	25.1	20.0	17.2	14.8	12.9	11.3	10.0	8.9	7.9	7.0	6.2	5.4	4.7
General Characteristics * (99% Chip Yield)														
Maximum Substrate Diameter (mm)—High-volume Production (>200k wafers/quarter)	300	300	300	300	300	450	450	450	450	450	450	450	450	450
Edge exclusion (mm)	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Front surface particle size (mm), latex sphere equivalent (A)	≤ 65	≤ 65	≤ 65	≤ 65	≤ 65	≤ 45	≤ 45	≤ 45	≤ 32	≤ 32	≤ 32	≤ 22	≤ 22	≤ 22
Particles (cm ⁻²)	≤ 0.33	≤ 0.33	≤ 0.32	≤ 0.15	≤ 0.15	≤ 0.32	≤ 0.16	≤ 0.16	≤ 0.31	≤ 0.16	≤ 0.16	≤ 0.33	≤ 0.17	≤ 0.17
Particles (#/wt)	≤ 220	≤ 220	≤ 210	≤ 105	≤ 105	≤ 400	≤ 240	≤ 240	≤ 490	≤ 240	≤ 240	≤ 510	≤ 250	≤ 250
Site flatness (mm), SFQR 26mm x 8 mm Site Size	≤ 68	≤ 59	≤ 52	≤ 45	≤ 40	≤ 36	≤ 32	≤ 28	≤ 25	≤ 23	≤ 20	≤ 18	≤ 16	≤ 14
Nanotopography, p-v, 2 mm dia. analysis area (I)	≤ 17	≤ 15	≤ 13	≤ 11	≤ 10	≤ 9	≤ 8	≤ 7	≤ 6	≤ 6	≤ 5	≤ 4	≤ 4	≤ 4
Epitaxial Wafer * (99% Chip Yield)														
Large structural epi defects (DRAM) (cm ⁻²) (B)	≤ 0.009	≤ 0.012	≤ 0.016	≤ 0.011	≤ 0.014	≤ 0.017	≤ 0.011	≤ 0.014	≤ 0.017	≤ 0.011	≤ 0.014	≤ 0.017	≤ 0.011	≤ 0.014
Large structural epi defects (MPU) (cm ⁻²) (B)	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004
Small structural epi defects (DRAM) (cm ⁻²) (C)	≤ 0.019	≤ 0.025	≤ 0.033	≤ 0.022	≤ 0.027	≤ 0.034	≤ 0.022	≤ 0.027	≤ 0.034	≤ 0.022	≤ 0.027	≤ 0.034	≤ 0.022	≤ 0.027
Small structural epi defects (MPU) (cm ⁻²) (C)	≤ 0.006	≤ 0.008	≤ 0.010	≤ 0.006	≤ 0.008	≤ 0.010	≤ 0.006	≤ 0.008	≤ 0.010	≤ 0.006	≤ 0.008	≤ 0.010	≤ 0.006	≤ 0.008
Silicon-On-Insulator Wafer * (99% Chip Yield)														
Edge exclusion (mm)	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Starting silicon layer thickness (Partially Depleted) (tolerance = 5%, 3σ) (mm) (D)	58-100	54-93	50-76	46-71	43-65	40-60	38-56	35-52	33-48	31-45	29-42	28-39	26-37	25-34
Starting silicon layer thickness (Fully Depleted) (tolerance = 5%, 3σ) (mm) (E)					16-20	15-19	15-18	14-16	13-16	13-15	13-15	13-14	12-14	12-14
Buried oxide (BOX) thickness (Fully Depleted) (tolerance = 5%, 3σ) (mm) (F)				36-60	34-56	30-50	28-46	26-42	24-38	22-36	20-32	18-30	16-26	14-24
D _{large} Large area SOI wafer defects (DRAM) (cm ⁻²) (G)	≤ 0.009	≤ 0.012	≤ 0.016	≤ 0.011	≤ 0.014	≤ 0.017	≤ 0.011	≤ 0.014	≤ 0.017	≤ 0.011	≤ 0.014	≤ 0.017	≤ 0.011	≤ 0.014
D _{large} Large area SOI wafer defects (MPU) (cm ⁻²) (G)	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004	≤ 0.005	≤ 0.003	≤ 0.004
D _{small} Small area SOI wafer defects (DRAM) (cm ⁻²) (H)	≤ 0.150	≤ 0.198	≤ 0.262	≤ 0.173	≤ 0.218	≤ 0.274	≤ 0.173	≤ 0.218	≤ 0.274	≤ 0.173	≤ 0.218	≤ 0.274	≤ 0.173	≤ 0.218
D _{small} Small area SOI wafer defects (MPU) (cm ⁻²) (H)	≤ 0.159	≤ 0.200	≤ 0.252	≤ 0.159	≤ 0.200	≤ 0.252	≤ 0.159	≤ 0.200	≤ 0.252	≤ 0.159	≤ 0.200	≤ 0.252	≤ 0.159	≤ 0.200

manufacturable solutions exist

manufacturable solutions known

manufacturable solutions unknown

* International Technology Roadmap for Semiconductors - 2008 Revision (<http://www.itrs.net/>)

Carbono e eletrônica: por que é interessante?

Propriedades desejadas:

Capacidade de suportar correntes altas, alta condução de calor, carbono é mais robusto que silício, alta mobilidade, geometria permite escalar agressivamente, etc..

Workshop on Maturity Evaluation for Selected “Beyond CMOS” Technologies, (San Francisco, CA, USA, July 12-13, 2008), co-sponsored by the National Science Foundation. Excerpts from the final report:

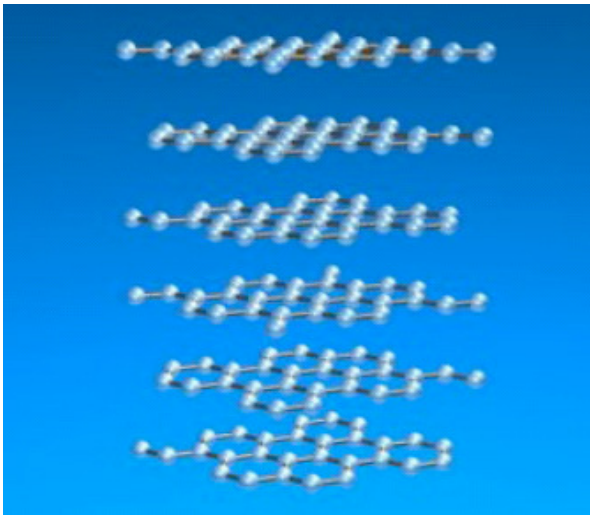
2008 Update: Working Group Summaries 29

The final outcome of this study is the ERD/ERM working groups chose Carbon-based Nanoelectronics as their recommended “Beyond CMOS” technology for accelerated development and more detailed roadmapping in the 2009 ITRS.

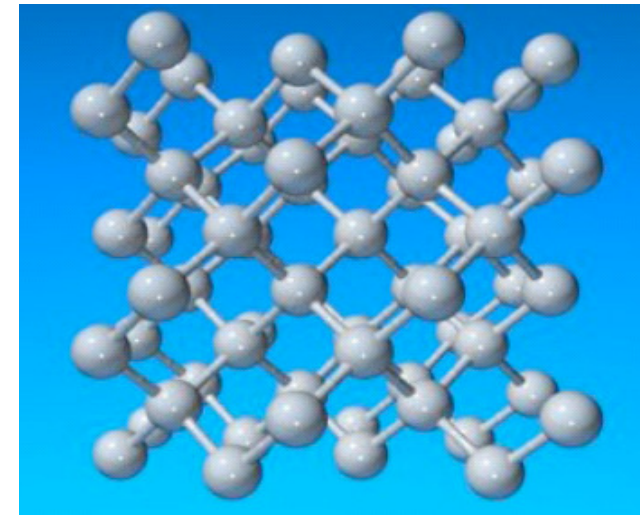
Carbon-based Nanoelectronics has a major advantage in that the science and technologies resulting from accelerated development of CNTs and GNRs for MOSFET applications can provide a substantial basis for exploring and developing new physical phenomena in these materials for “Beyond CMOS” information processing paradigms. The field of

Formas de ligação de carbono

grafite

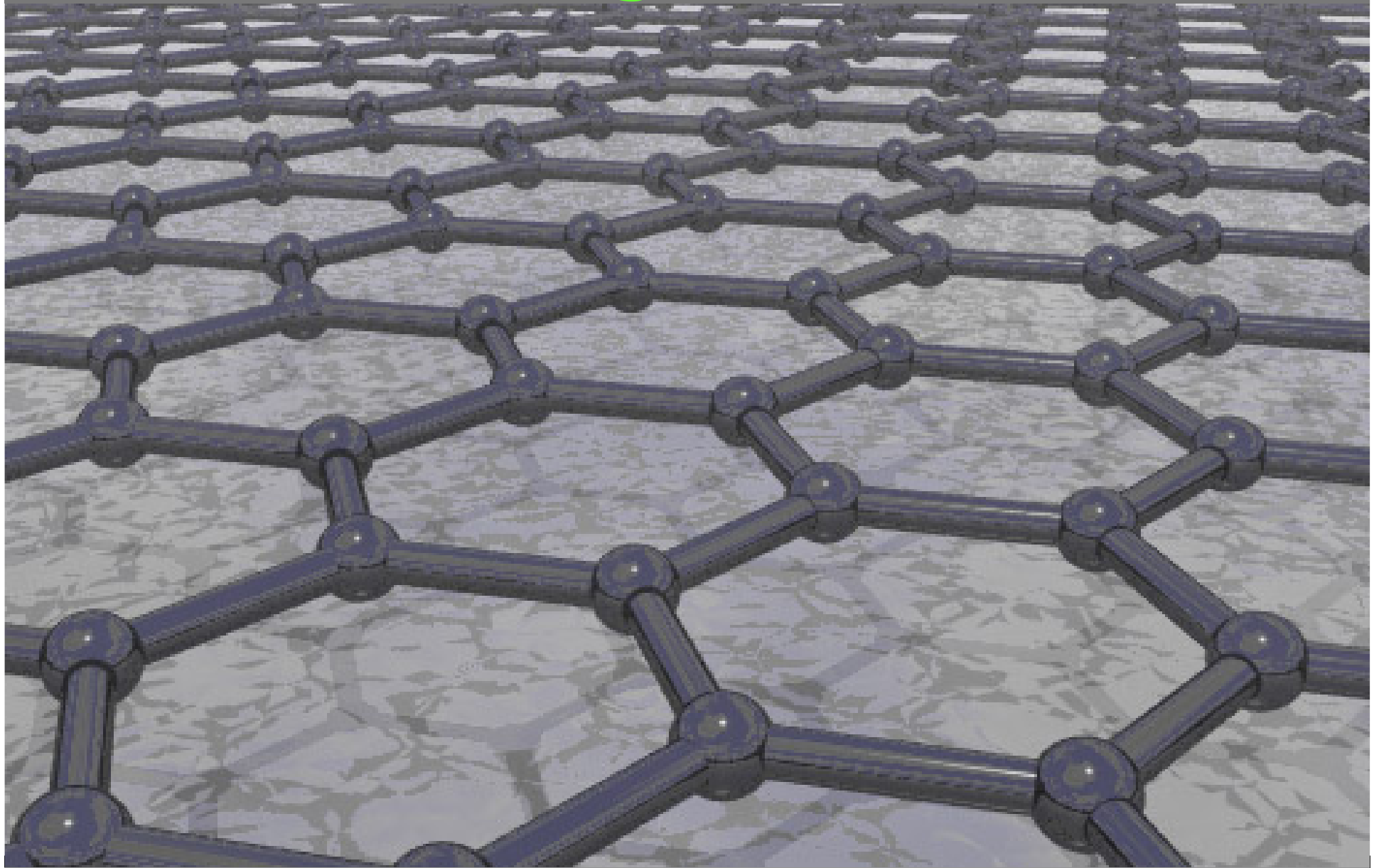


diamante



**Ligação flexível:
riqueza de estruturas**

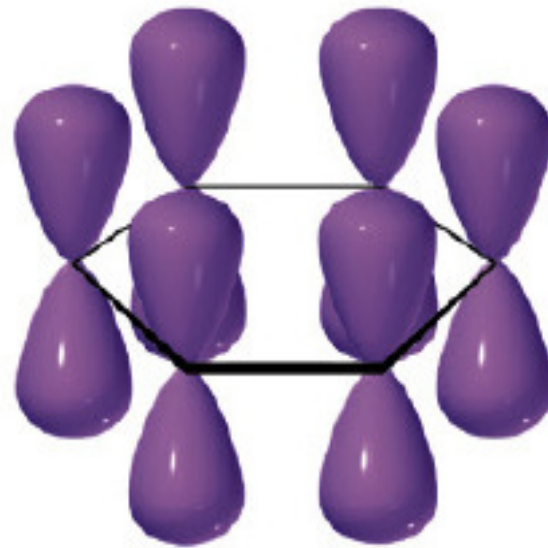
Personagem central



Grafeno

Elemento de construção: molécula de benzeno

estados p



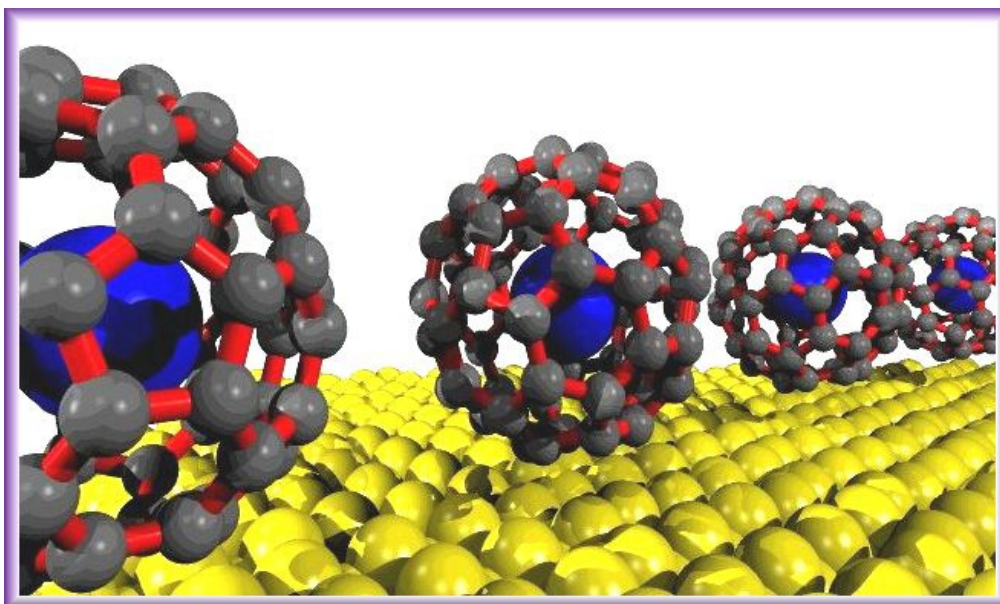
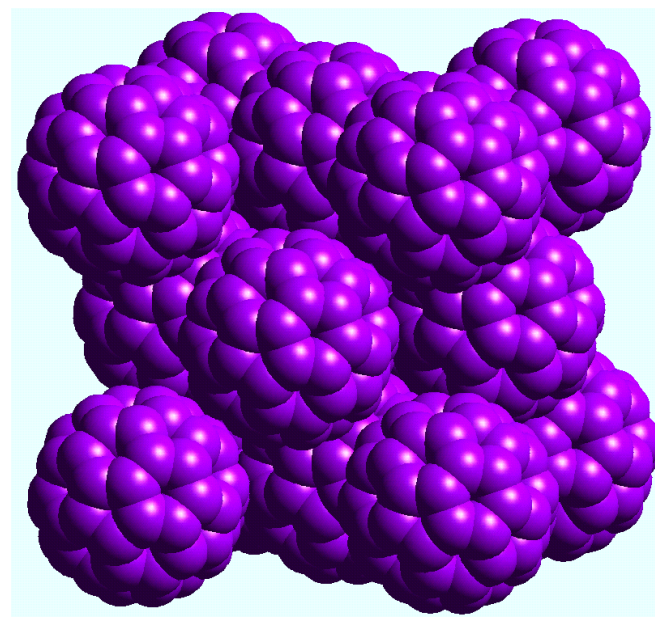
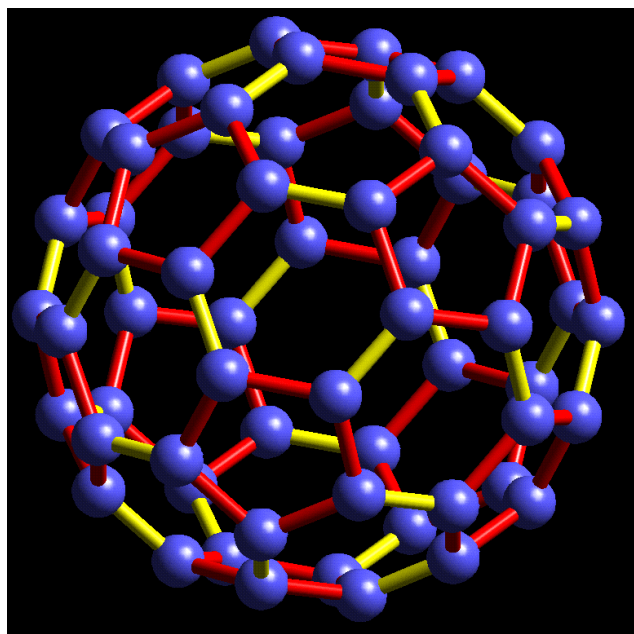
(a)

estado π



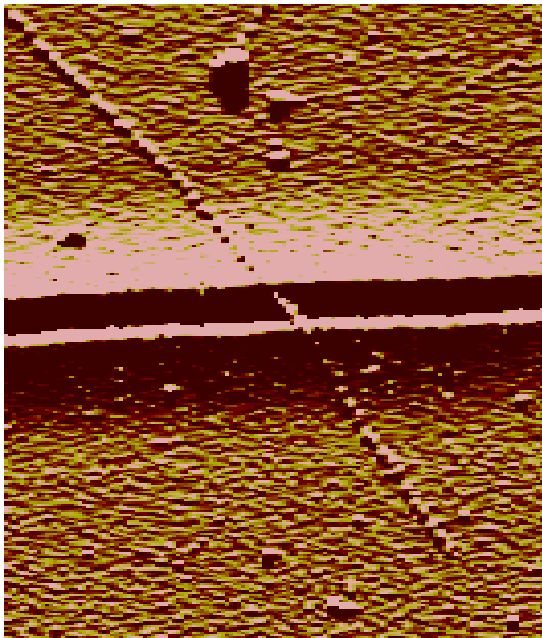
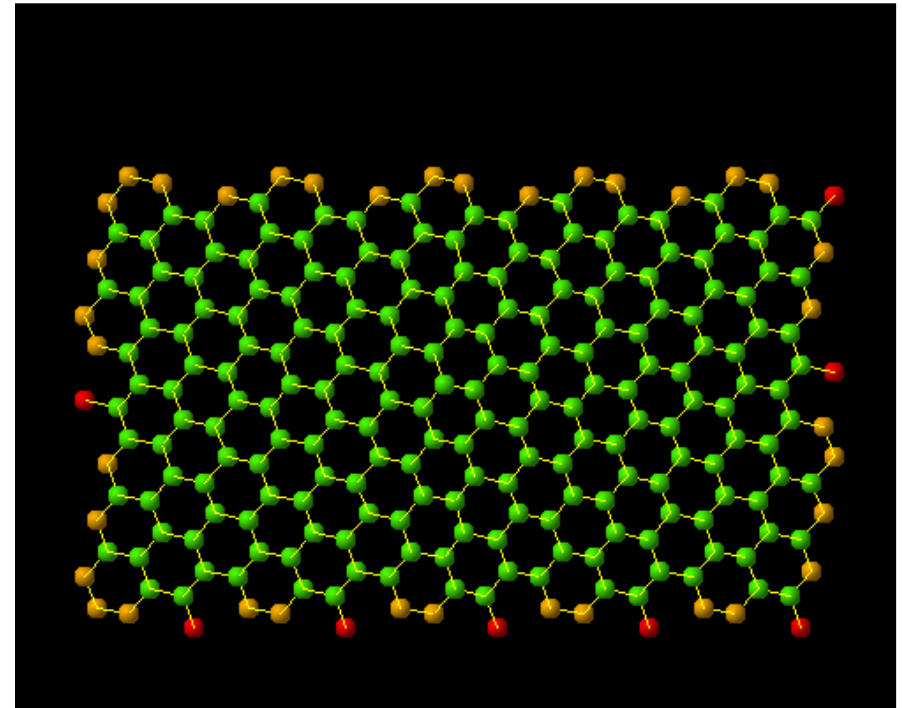
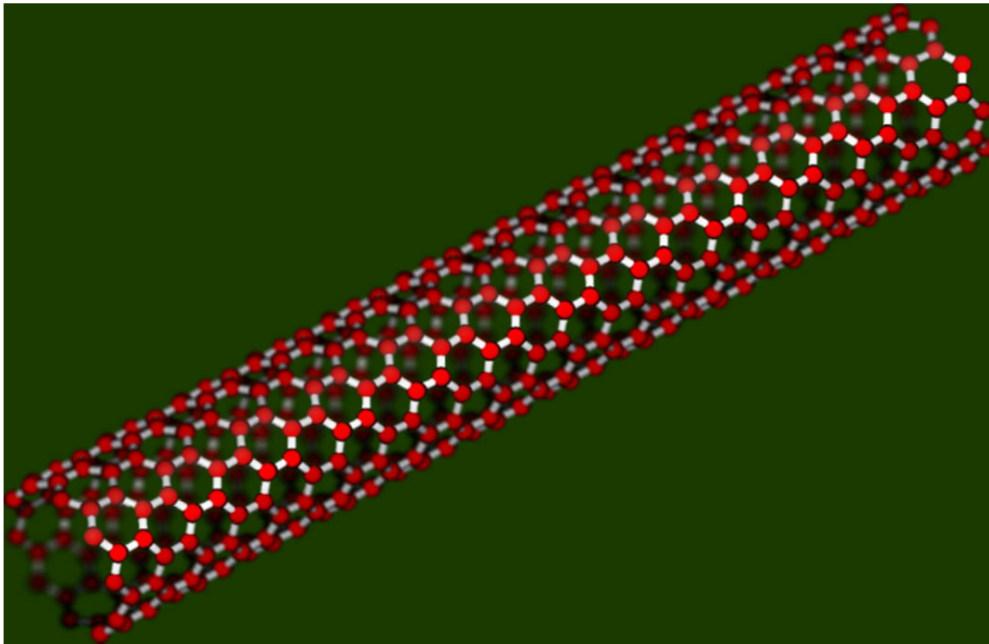
(b)

Linus Pauling, The nature of the chemical bond, pg 234-235 (1957)



**dimensão zero:
fulerenos**

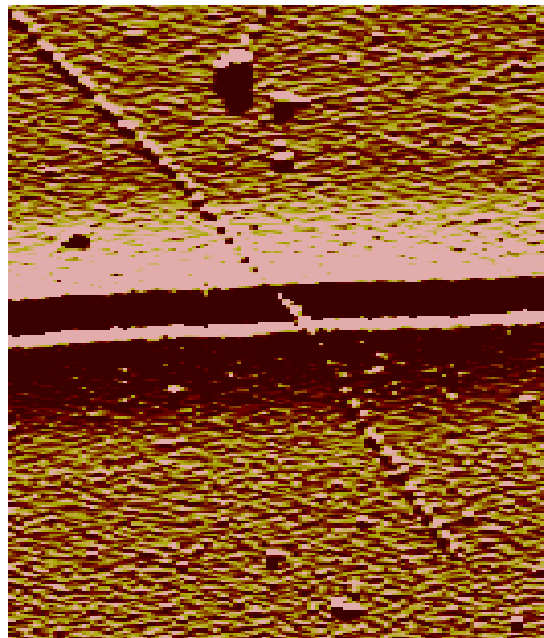
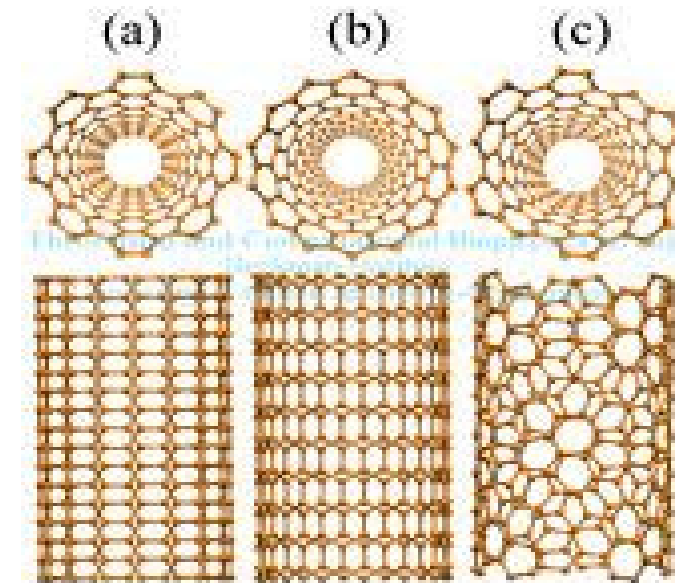
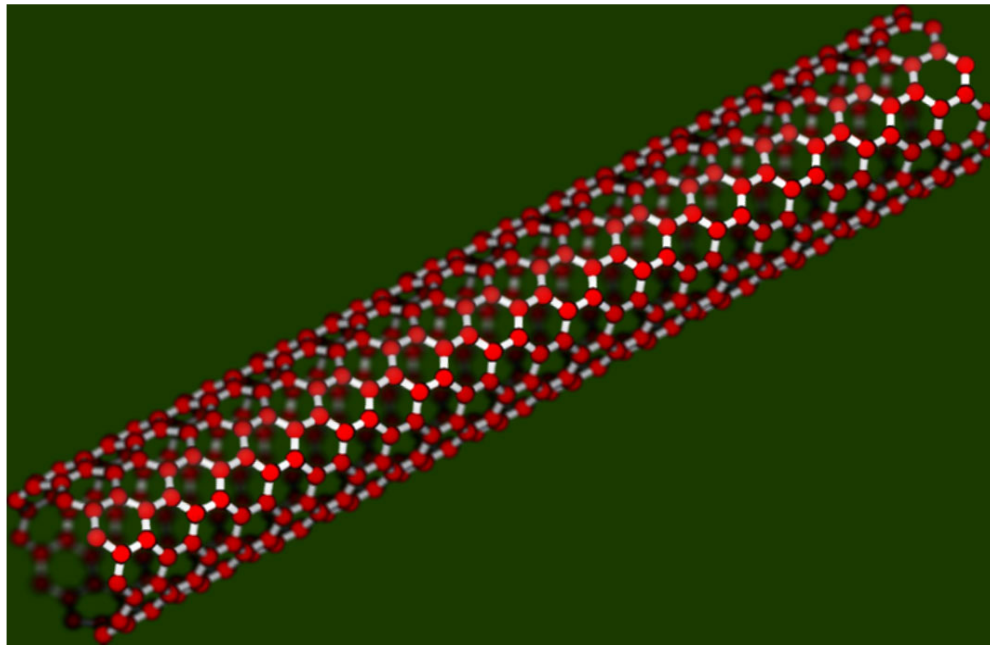
grafeno dobrado



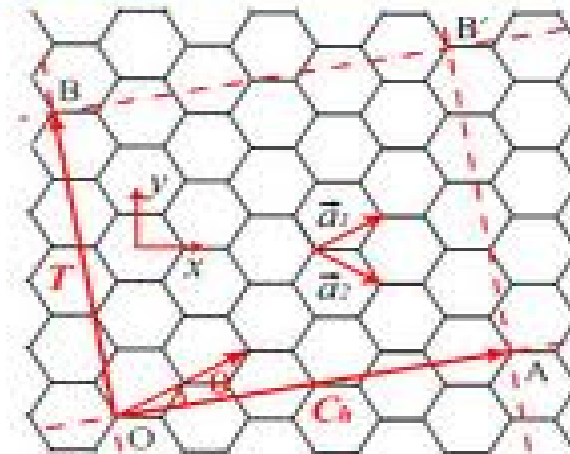
1 μm

**Unidimensional:
nanotubos de carbono**

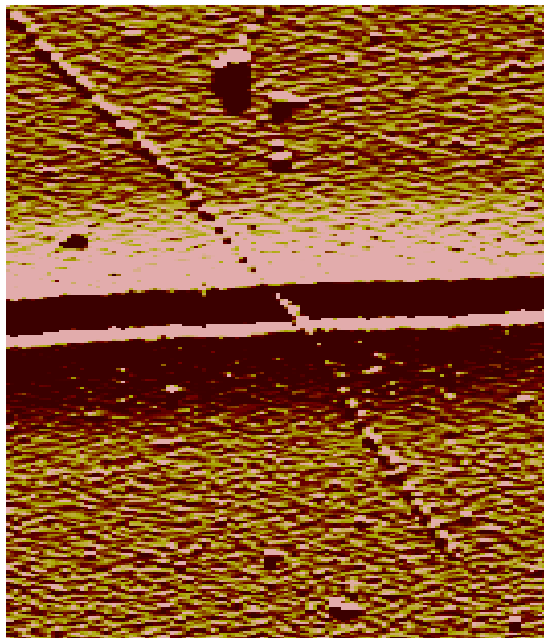
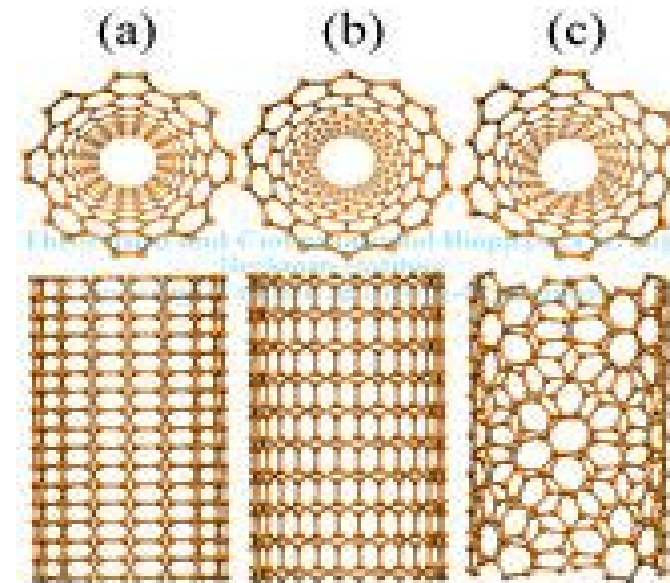
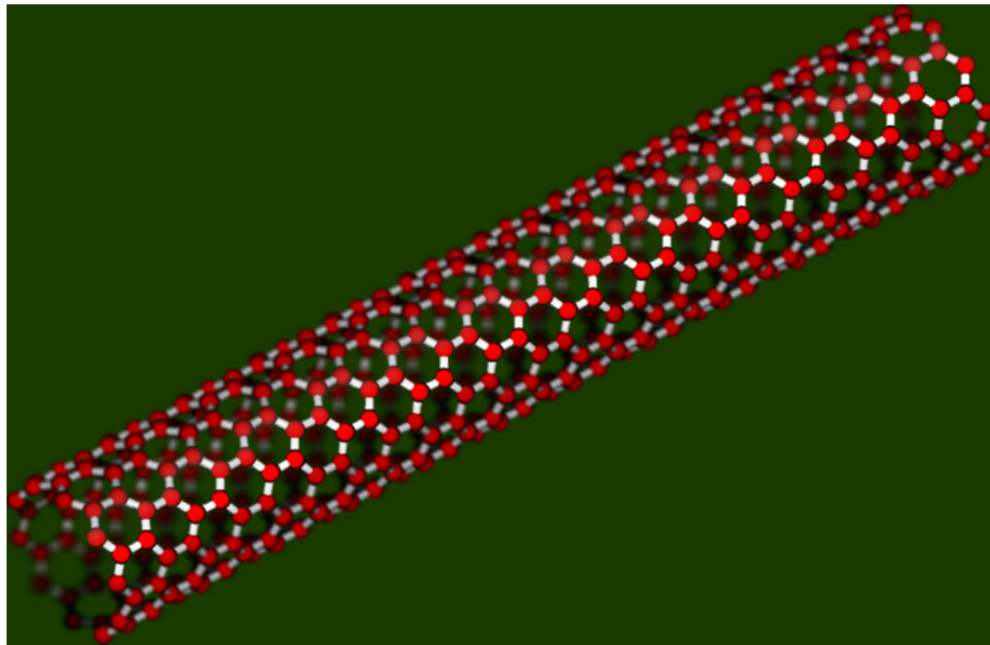
Grafeno enrolado



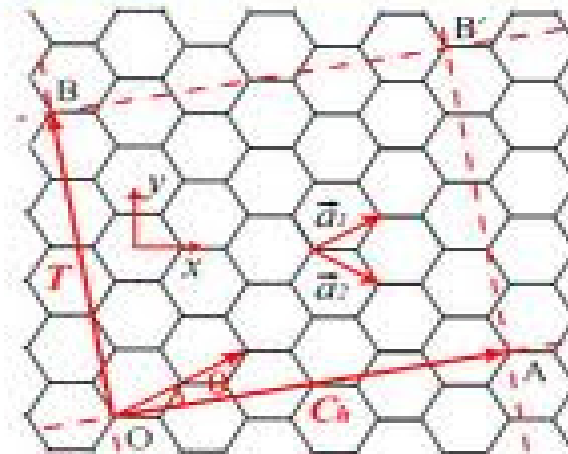
1 μm



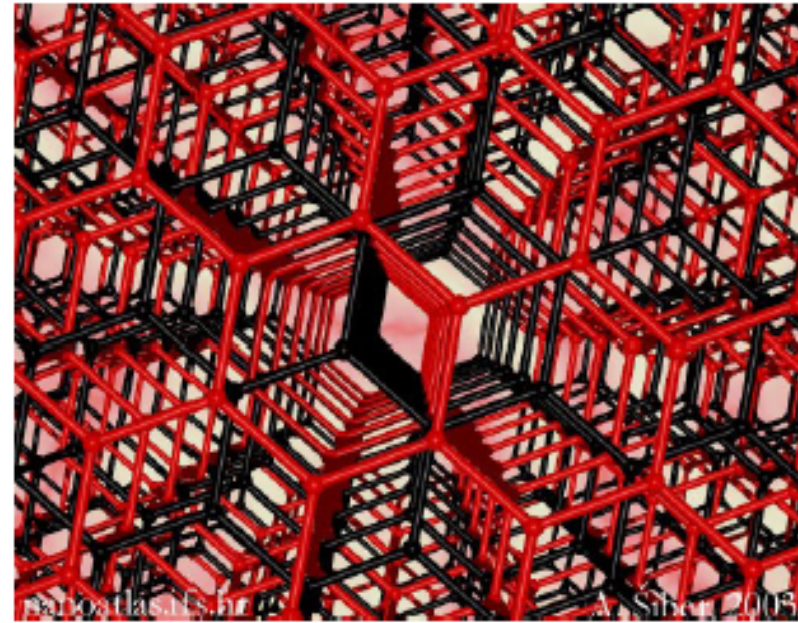
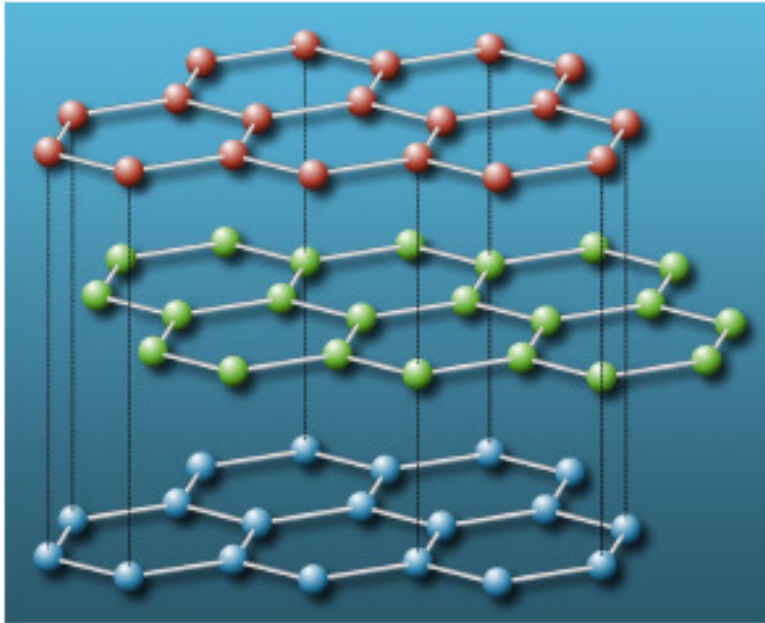
**Unidimensional:
nanotubos de carbono**



1 μm



grafeno enrolado



Tridimensional: grafite
grafeno empilhado

**Grafeno é o pai
de todos eles.**

Teoria de 60 anos.

PHYSICAL REVIEW

VOLUME 71, NUMBER 9

MAY 1, 1947

The Band Theory of Graphite

P. R. WALLACE*

National Research Council of Canada, Chalk River Laboratory, Chalk River, Ontario

(Received December 19, 1946)

Exercício

BAND THEORY OF GRAPHITE.

623

2. ZONE STRUCTURE OF A SINGLE HEXAGONAL LAYER

Since the spacing of the lattice planes of graphite is large (3.37Å) compared with the hexagonal spacing in the layer (1.42Å), a first approximation in the treatment of graphite may be obtained by neglecting the interactions between planes, and supposing that conduction takes place only in layers.

Graphite possesses four valence electrons. Three of these form tight bonds with neighboring atoms in the plane. Their wave functions are of the form

$$\frac{1}{\sqrt{3}}(\psi_c(2s) + \sqrt{2}\psi_c(\sigma_i 2p)) \quad (i=1, 2, 3),$$

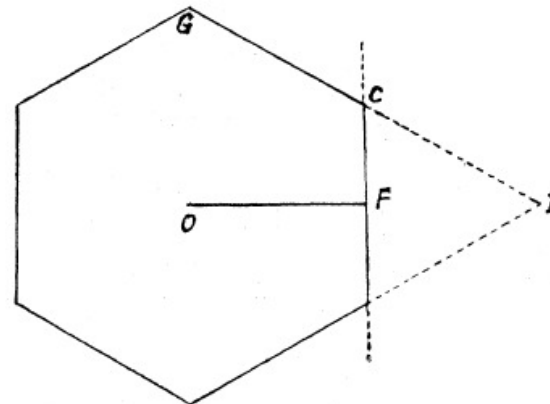
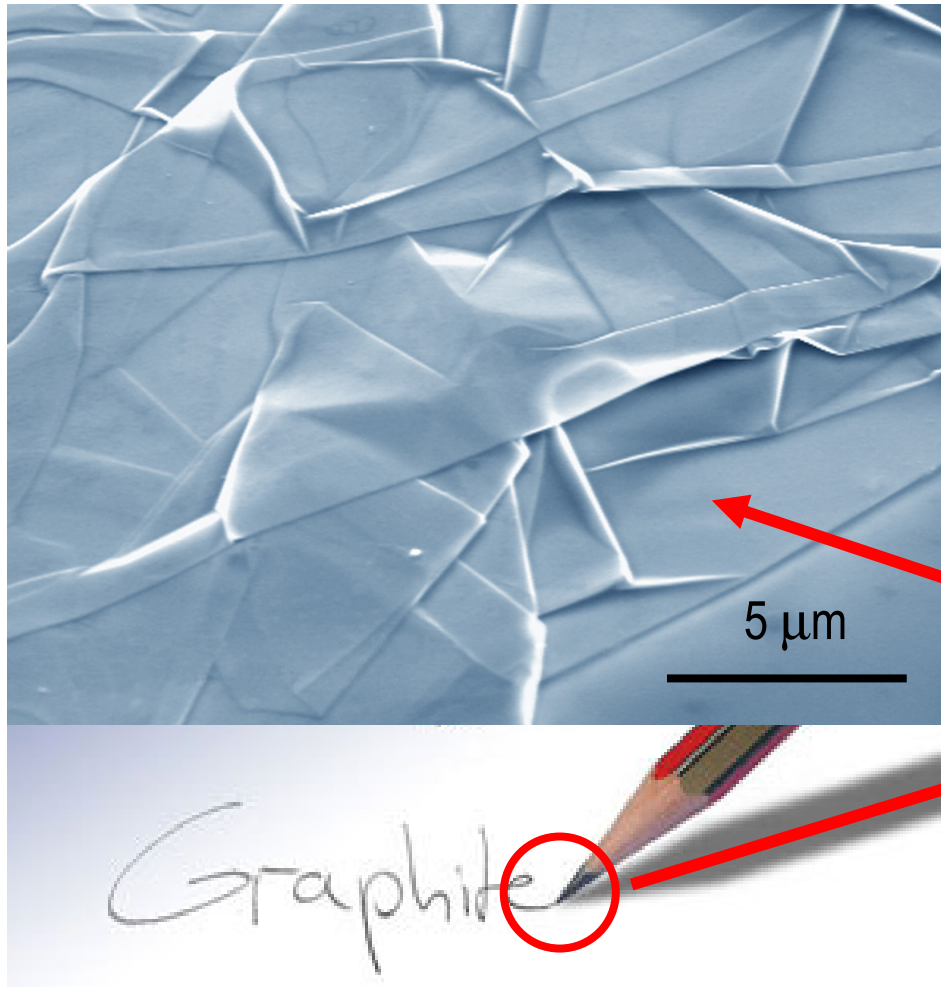


FIG. 2.

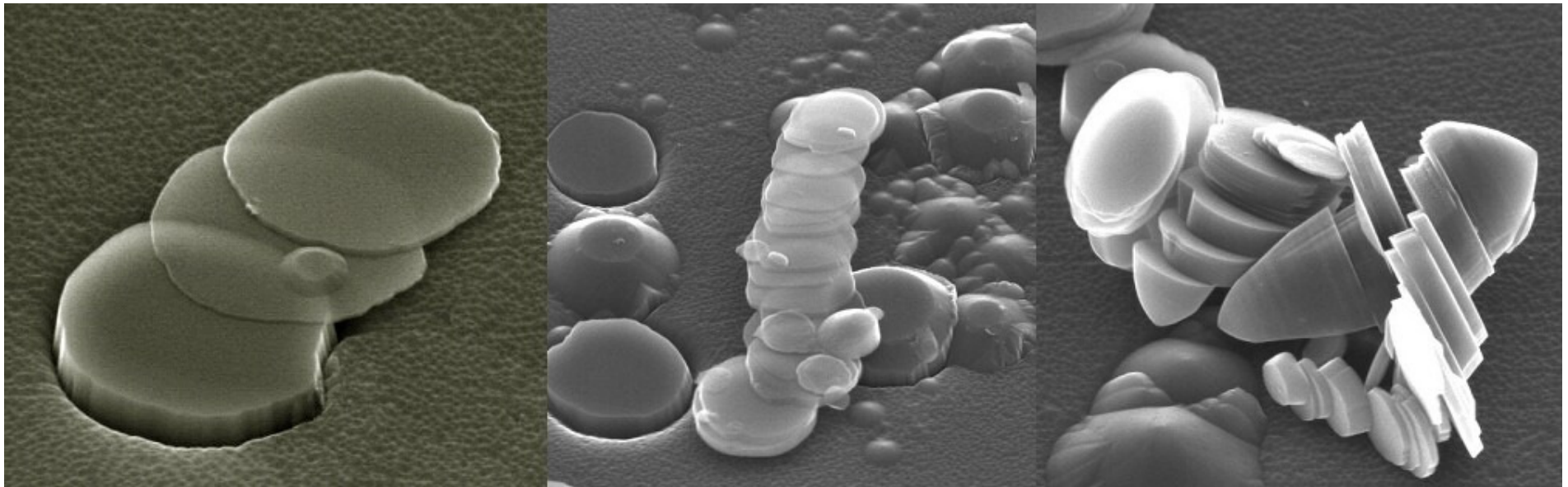
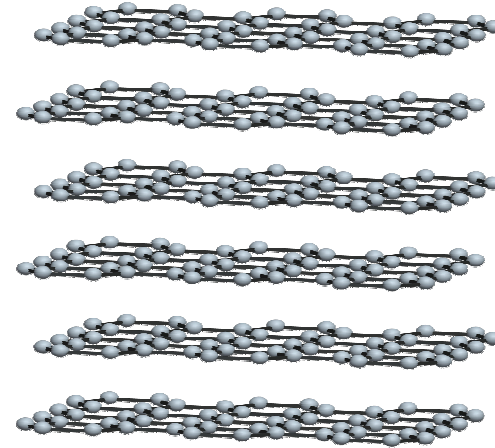
hexagon (Fig. 2) whose sides are distant $1/\sqrt{3}a$ from its center. It is easily shown that this zone contains one electron per atom, for the density

Grafeno: fácil de fazer, difícil de achar

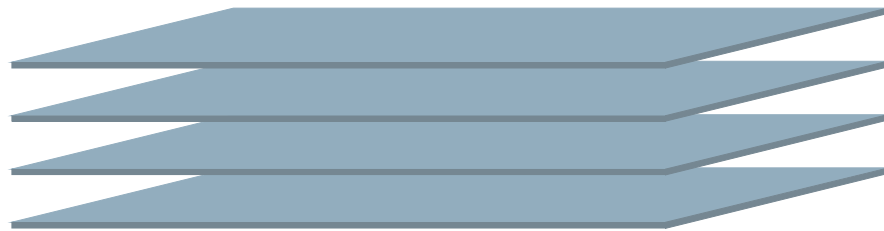


Quão fino podemos fatiar grafite?

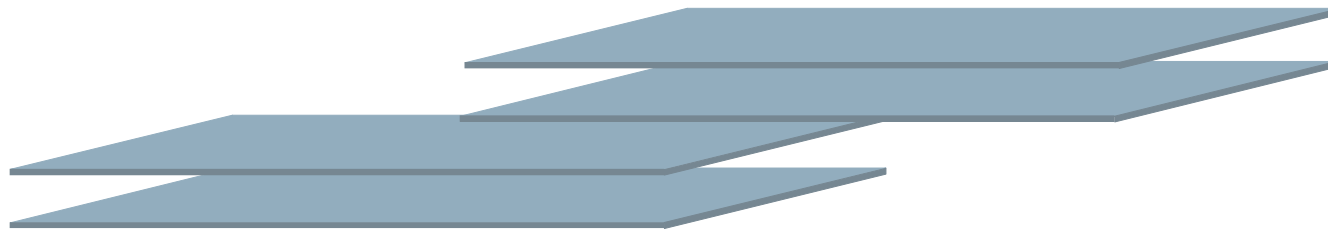
Estrutura de camadas do grafite



Podemos isolar uma única camada?



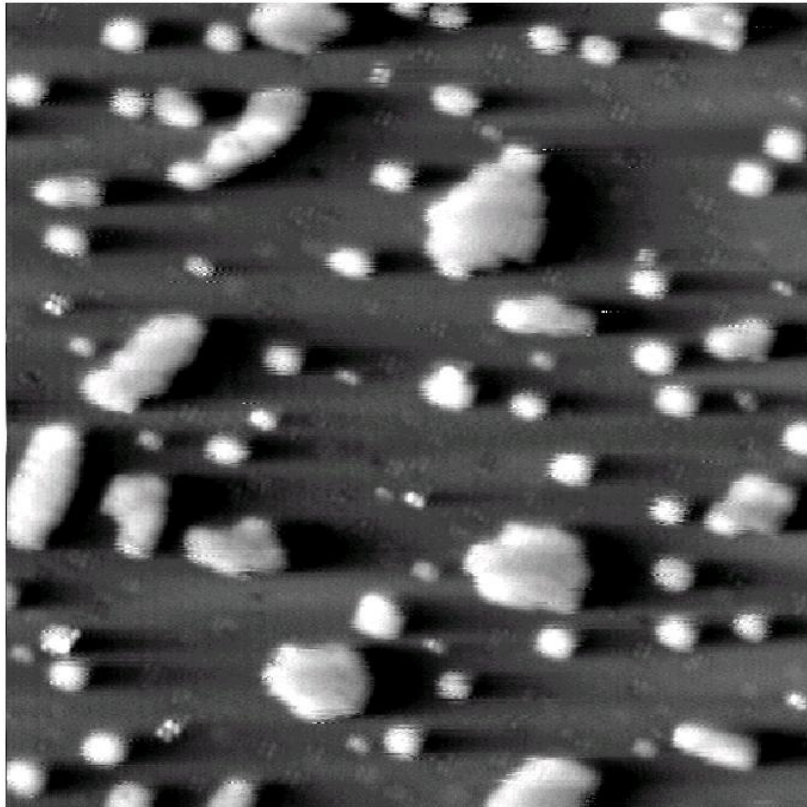
MATERIAL MULTI-CAMADAS



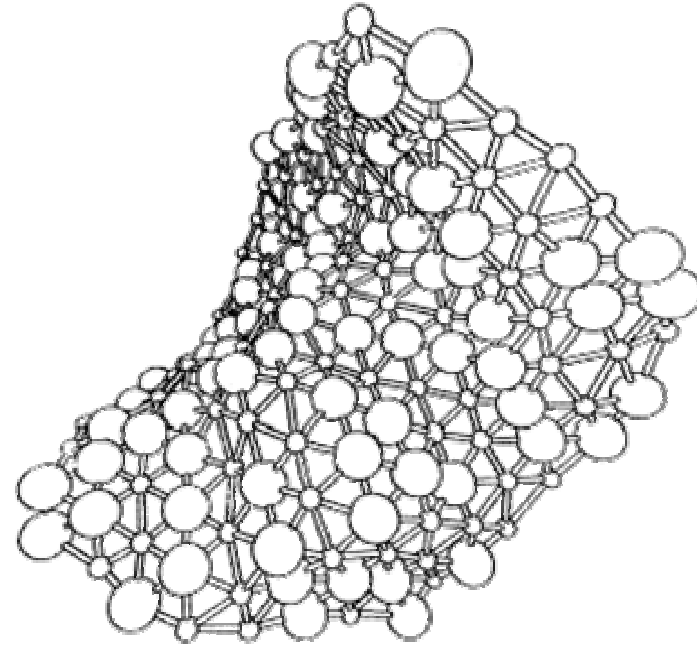
FATIAR ATÉ UM
ÚNICO PLANO?



A natureza “odeia” baixas dimensões



“crescimento de ilhas”
aglomerados de filmes finos

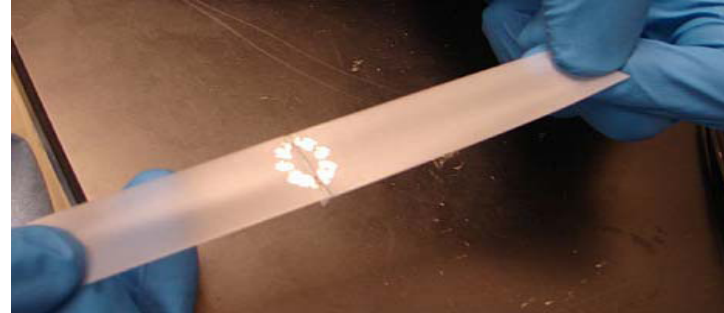
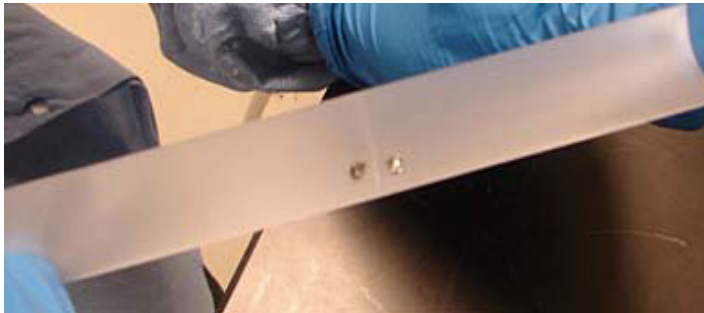


Precursores de 2D rapidamente
formam estruturas 3D

Peierls; Landau; Mermin-Wagner;

Clivagem mecânica

“Descascando” camadas de grafite com fita adesiva



Transferência
para
substrato
(em geral
 SiO_2)

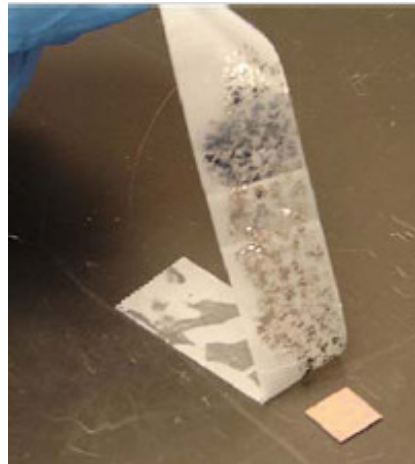
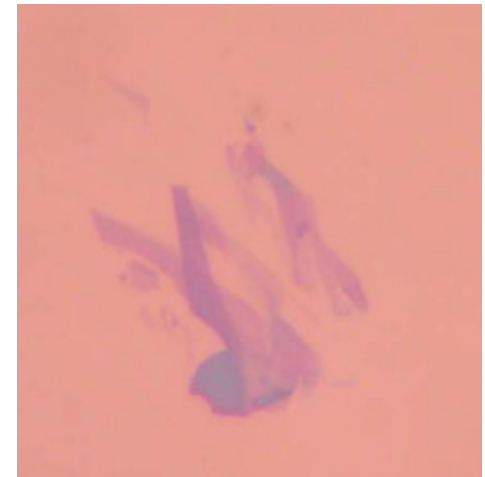
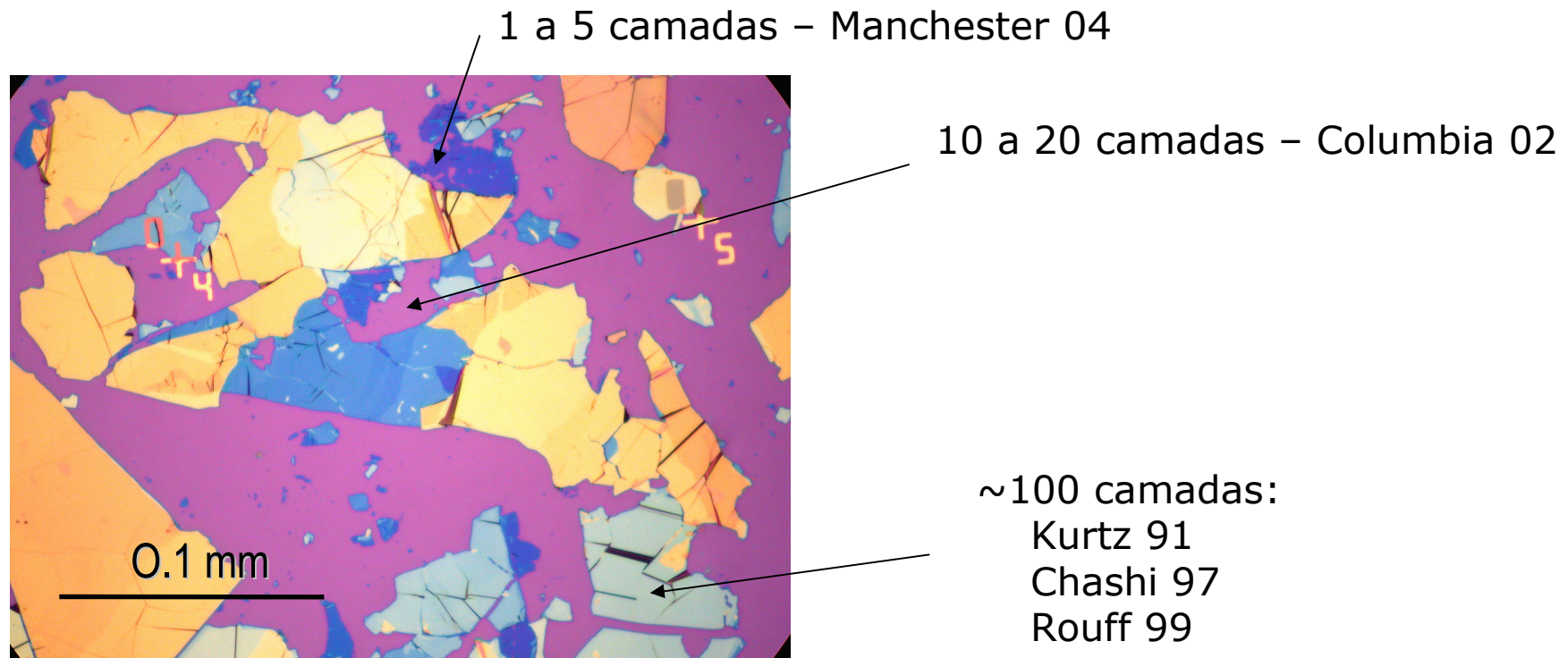


Imagem de
microscópio
ótico
dos flocos
resultantes

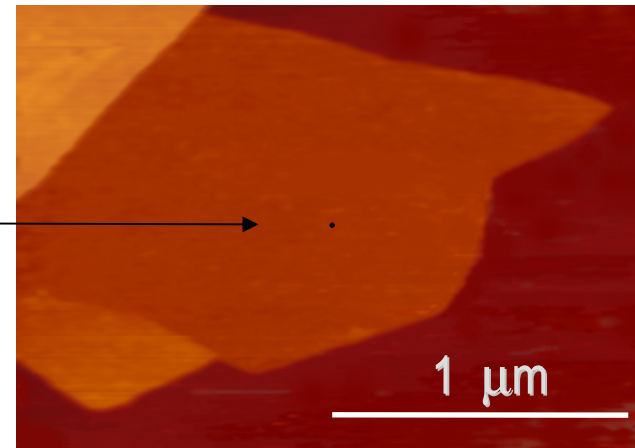
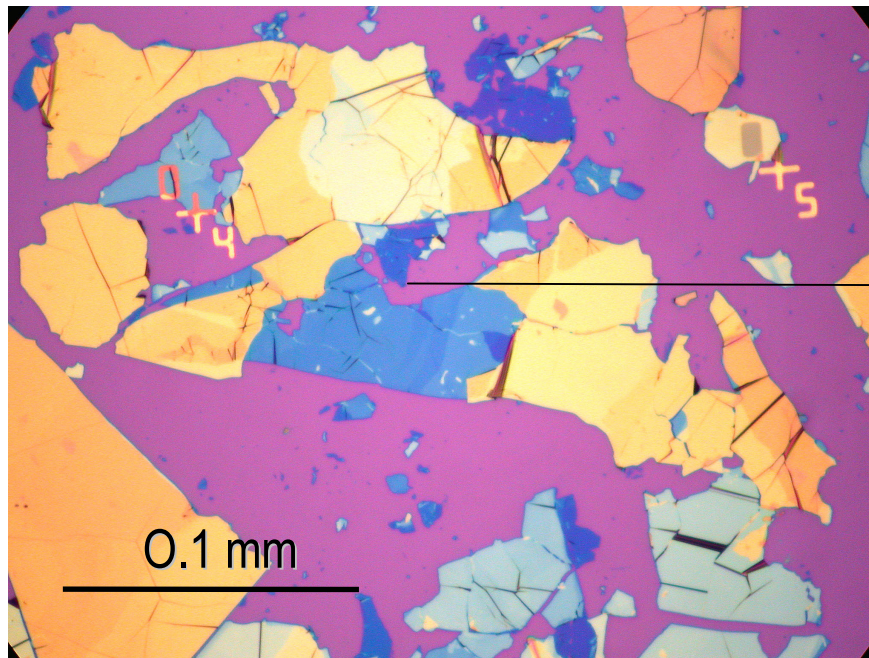


Técnica da “fita adesiva”



traços de grafite em um substrato de Si oxidado

Quão fino pode ser?

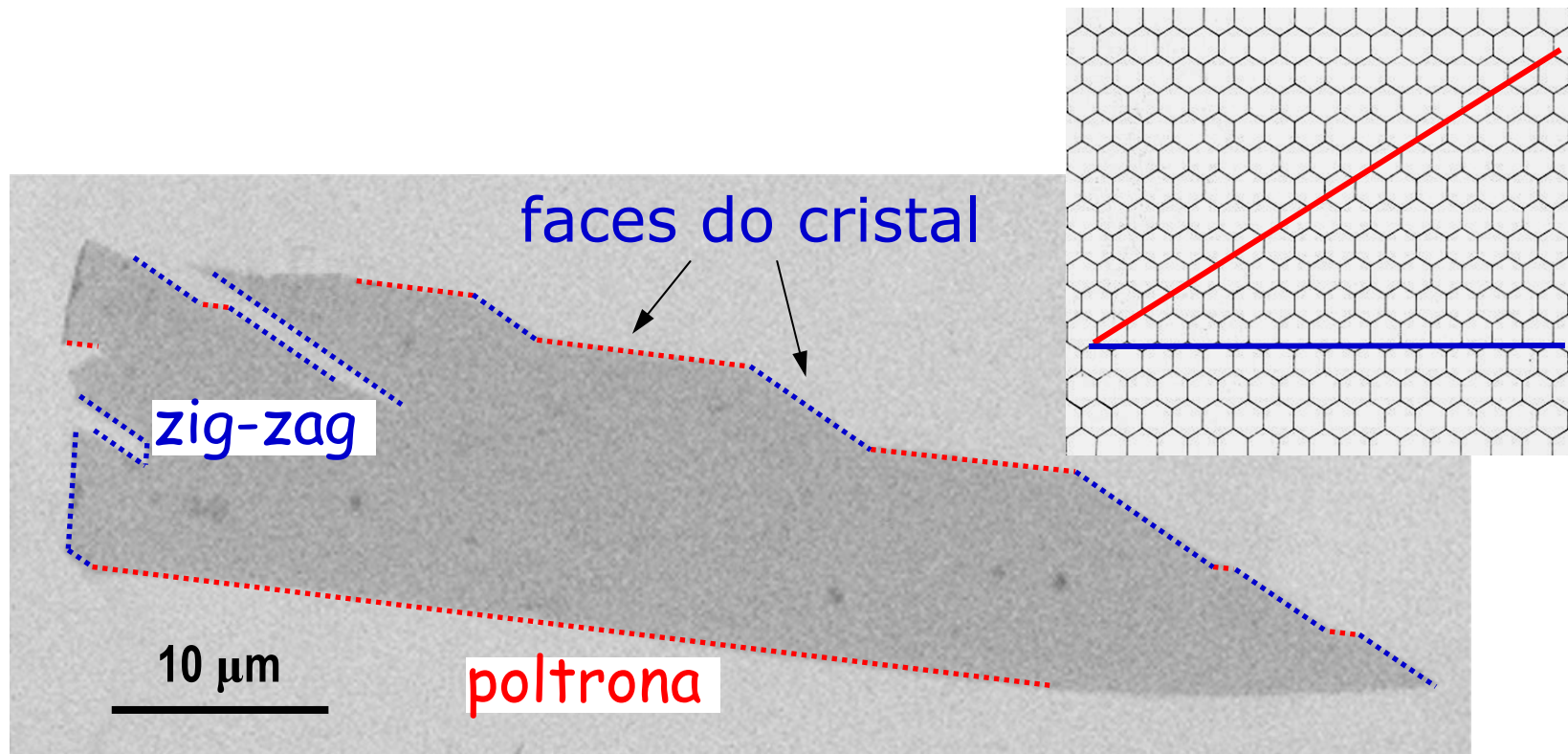


Grafeno – primeiramente demonstrado

Grupo de Manchester, *Science* '04

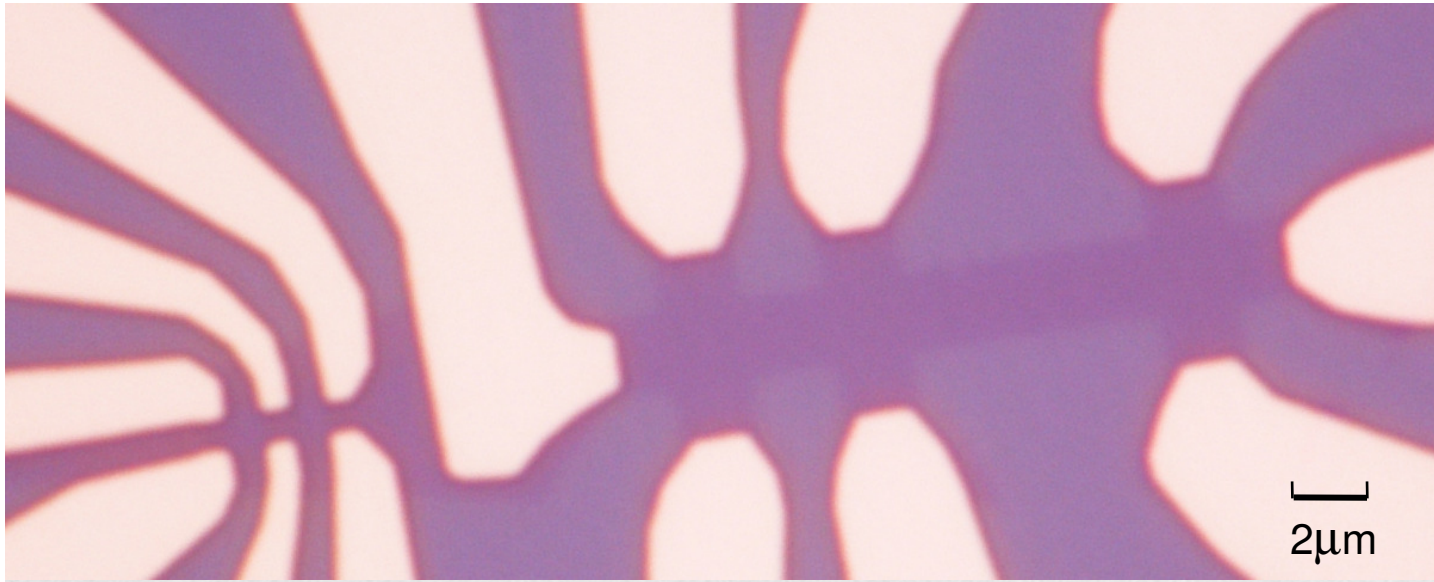
traços de grafite em um substrato de Si oxidado

Estado da arte

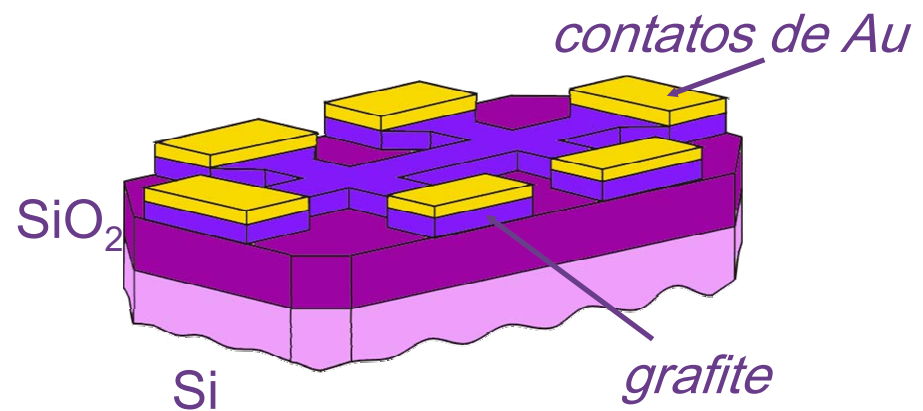


cristais 2D de grafeno

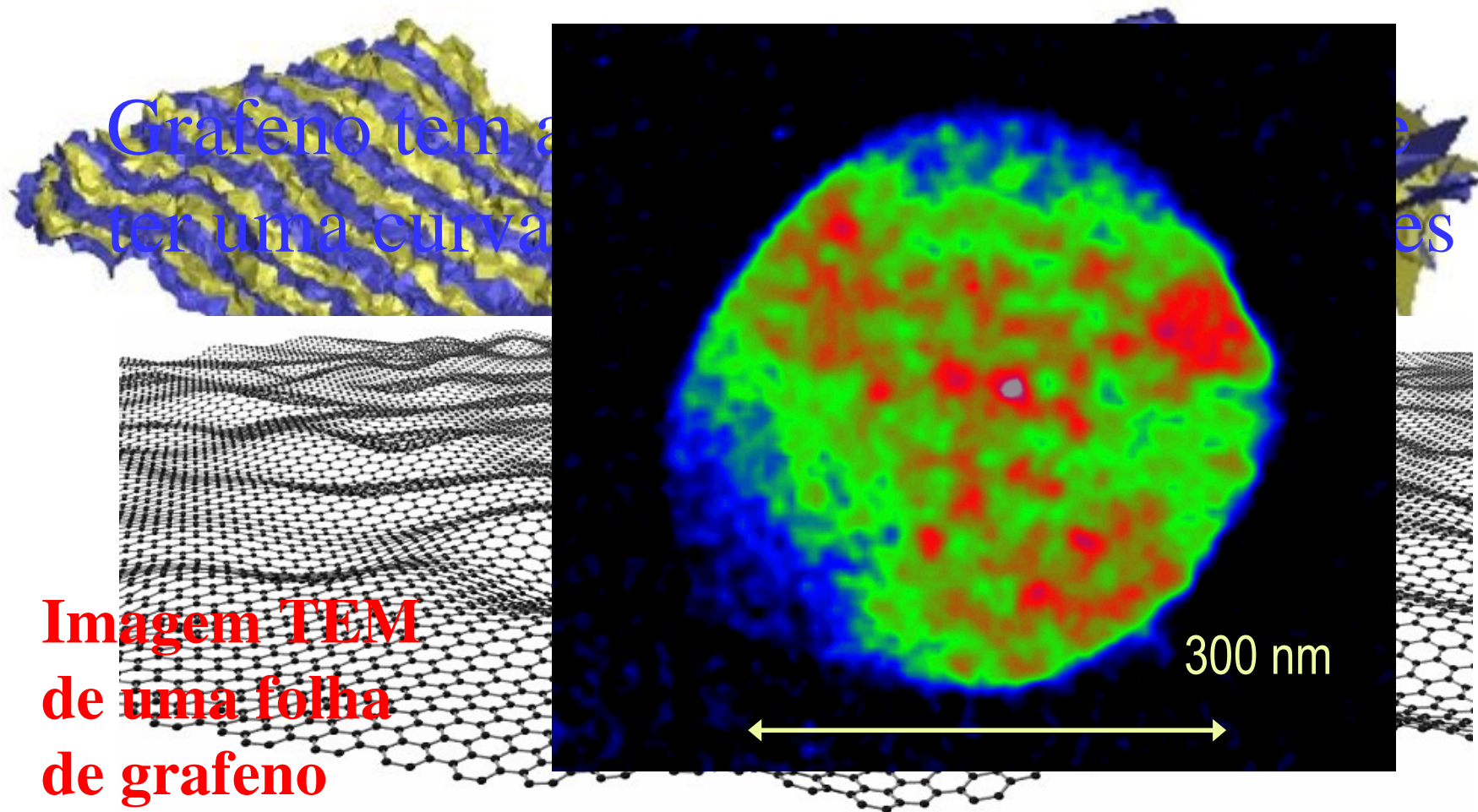
Estado da arte



- imagem ótica
- imagem MEV
- desenho
- contatos e suporte

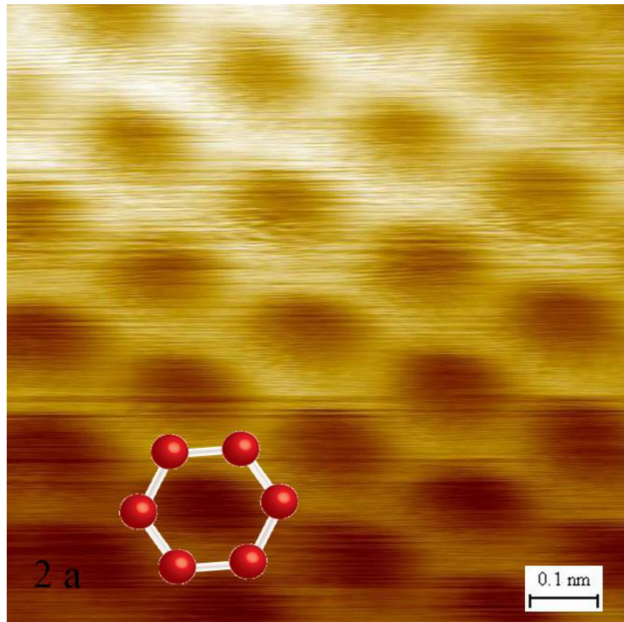


Grafeno tem a espessura de um átomo e é "mole"

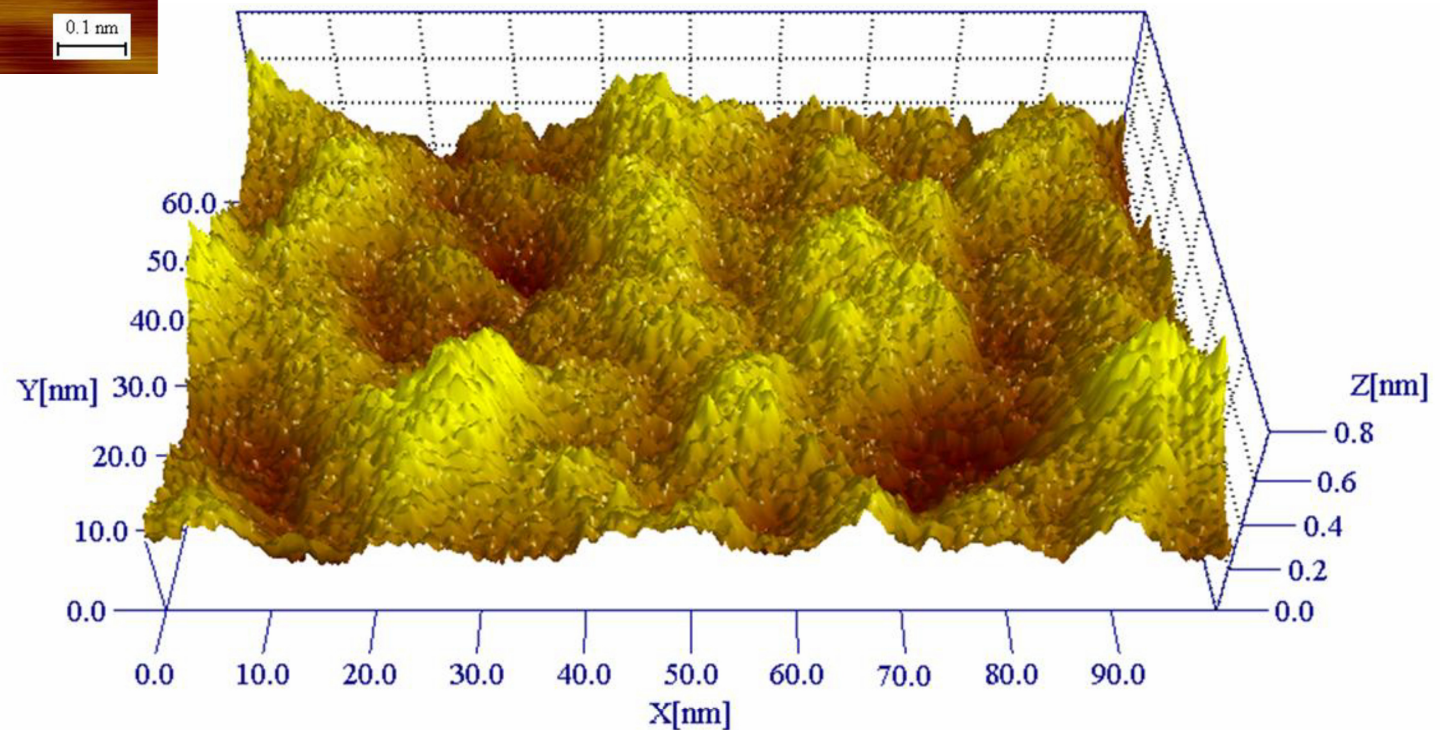


J. C. Meyer *et al.*, Nature **446**, 60 (07)

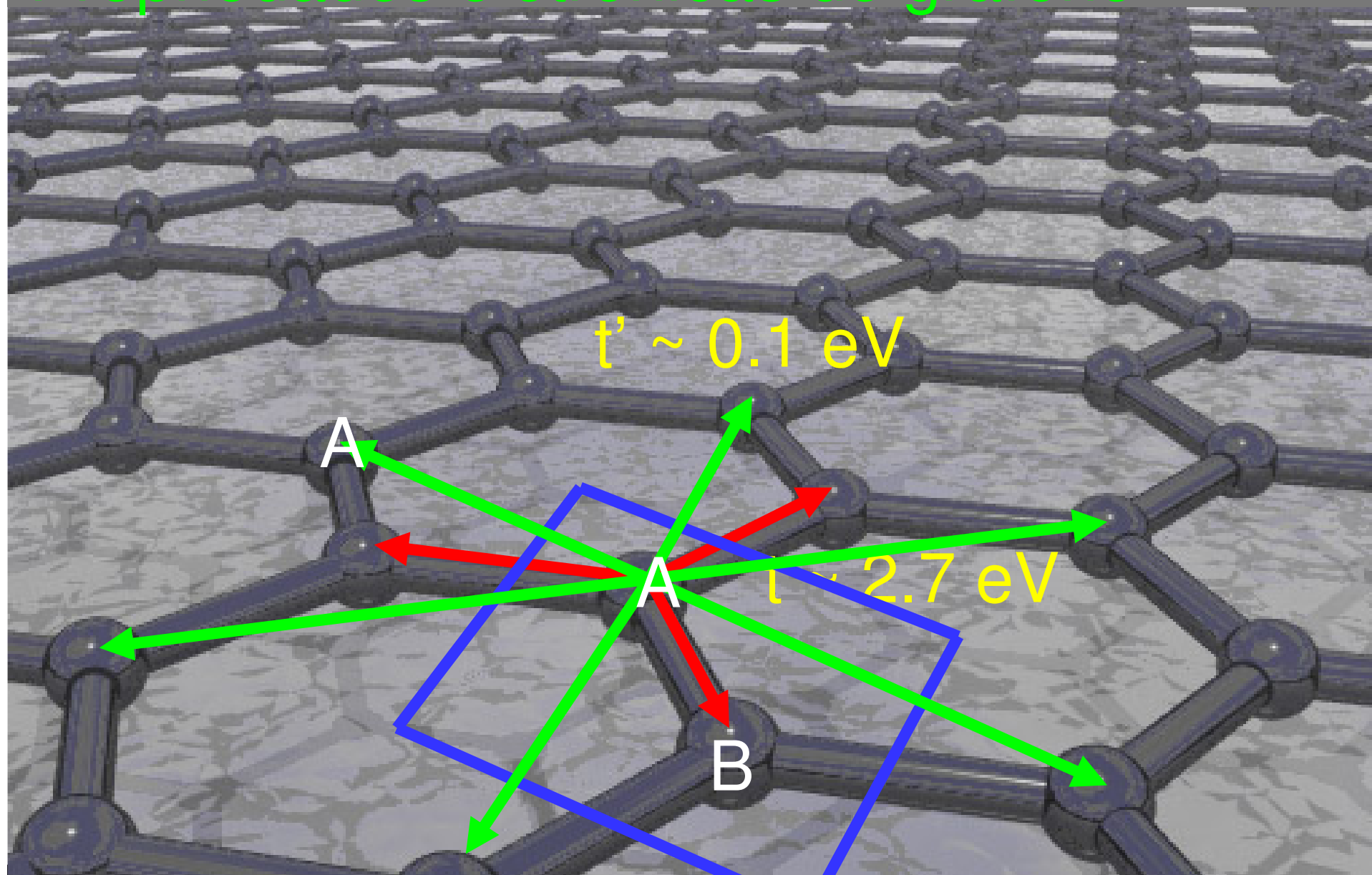
Microscopia de tunelamento



E. Stolyarova et al., PNAS 104, 9209 (2007)
Ishigami et al., Nano Letters (2007)

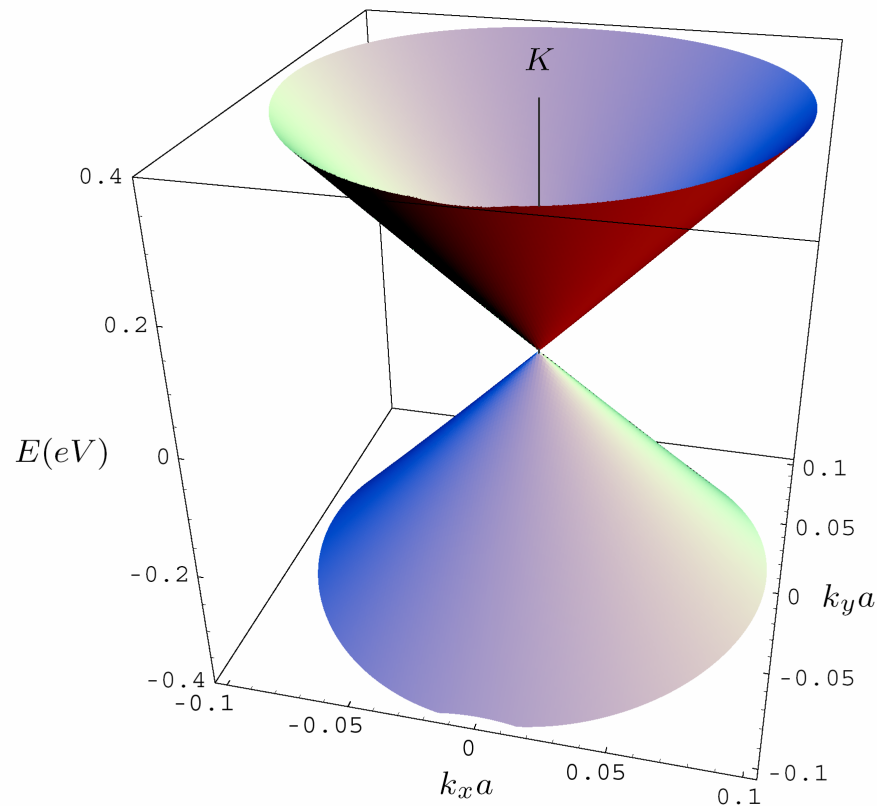


Propriedades eletrônicas do grafeno



Célula unitária Segundos vizinhos Primeiros vizinhos

Espaço de momentos



Cone de Dirac

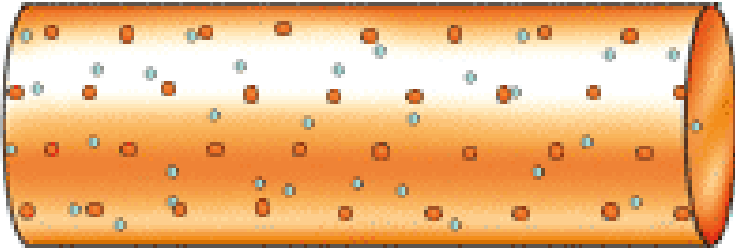
$$E_{\pm}(p) = \pm v_F \sqrt{p_x^2 + p_y^2} = \pm v_F p$$

$$E_{\pm}(p, m) = \pm \sqrt{m^2 v_F^4 + v_F^2 p^2} \quad \text{with } m = 0$$

$$v_F = \frac{3ta}{2} \approx c/300$$

**Estado sólido “ultra-relativístico”
com uma velocidade da luz baixa**

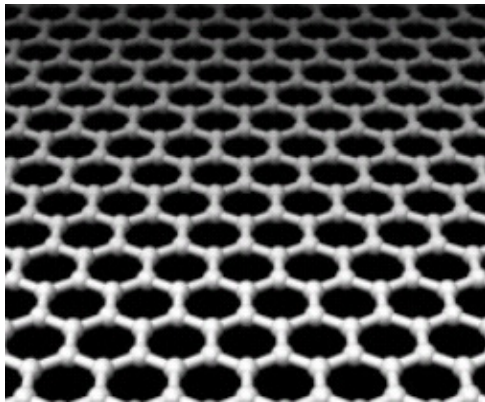
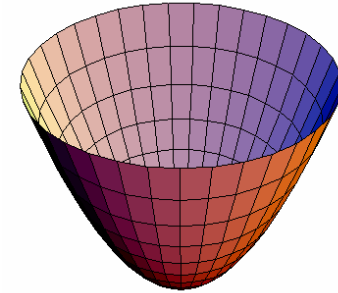
O que é tão especial em grafeno?



condutor normal

$$E(p) = \frac{p^2}{2m}$$

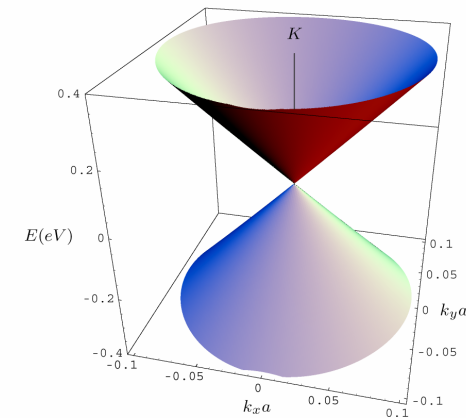
fermions



grafeno

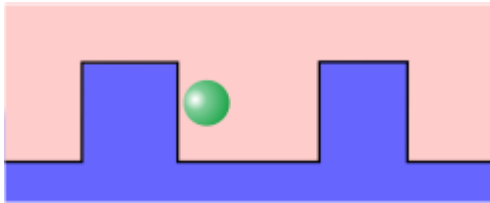
$$E(p) = \pm vp$$

fermions de
Dirac



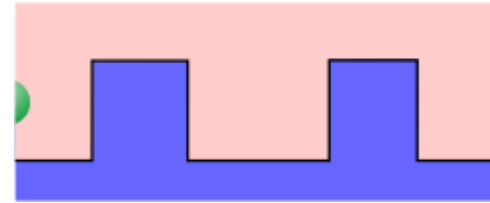
Paradoxo de Klein

partículas massivas em 1D:

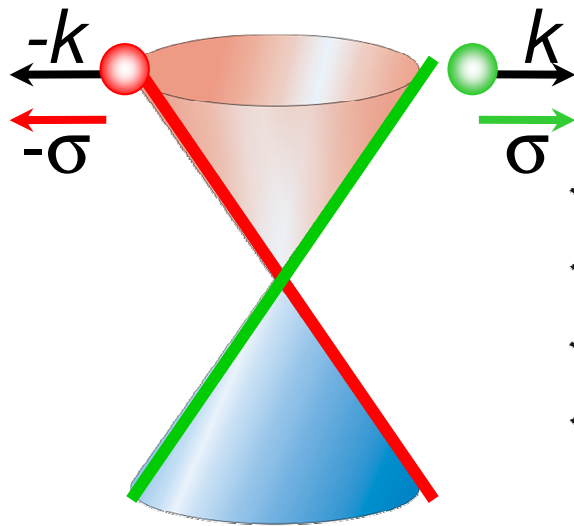


sempre localizadas

partículas sem massa em 1D:

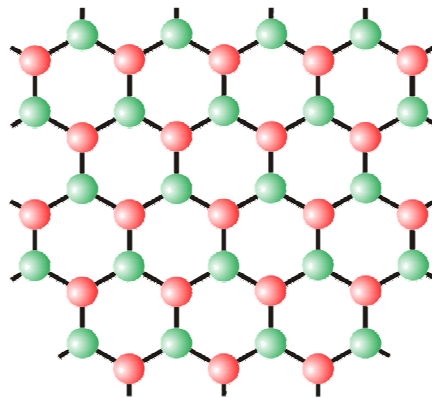


NUNCA LOCALIZADAS



propagação de partícula relativística
através de uma barreira

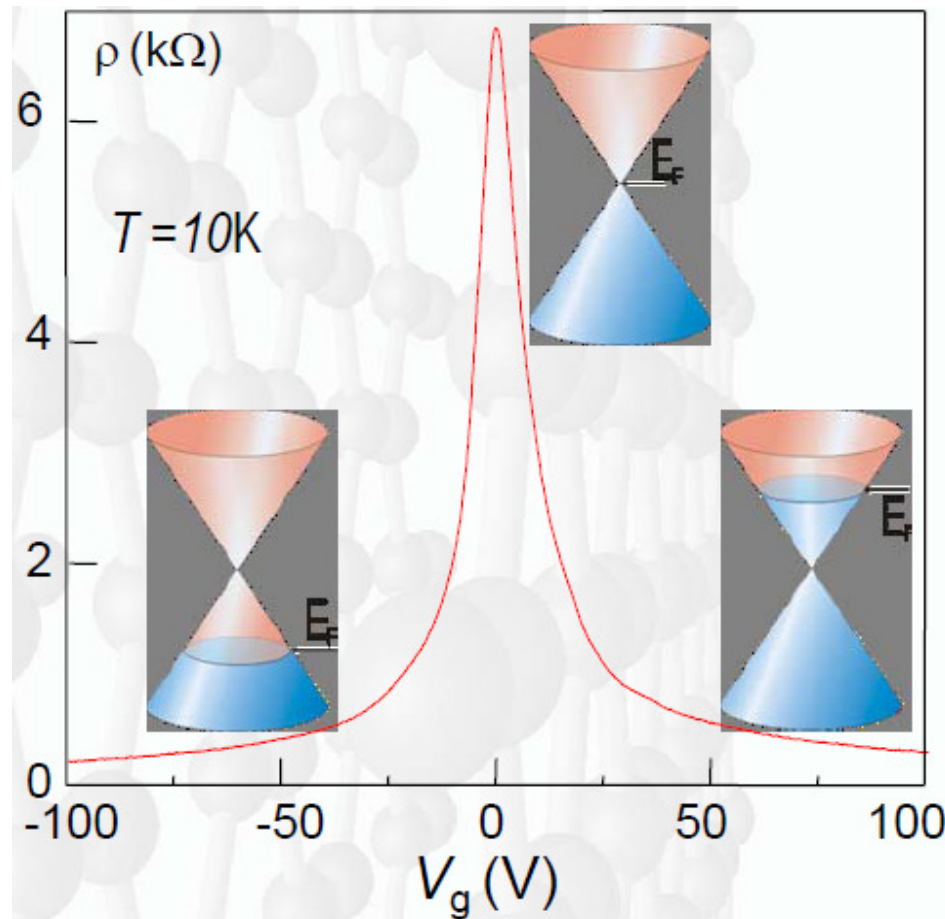
O. Klein, *Z. Phys* **53**,157 (1929); **41**, 407 (1927)



consequência da
conservação de
pseudo-spin

M.I.Katsnelson *et al*
Nature Physics 2006

Resistividade limitada por efeitos quânticos



*Atual mobilidade de portadores
até $\sim 15.000 \text{ cm}^2/\text{V.s}$ a $300K$
mesmo com alta dopagem*

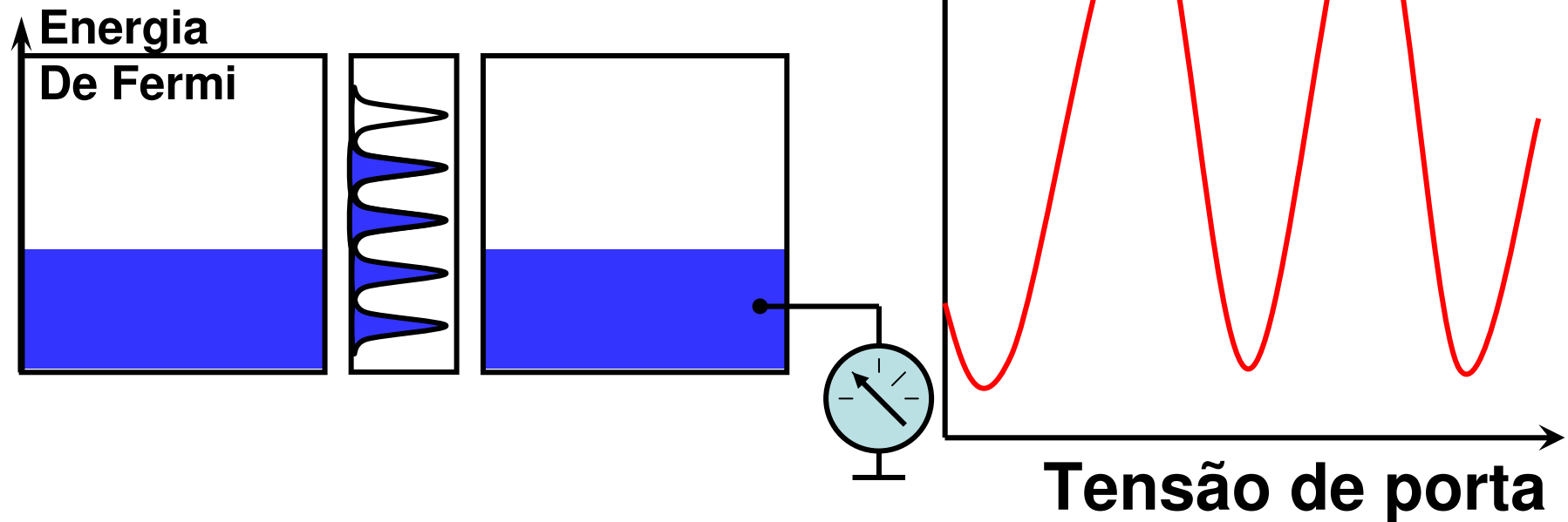
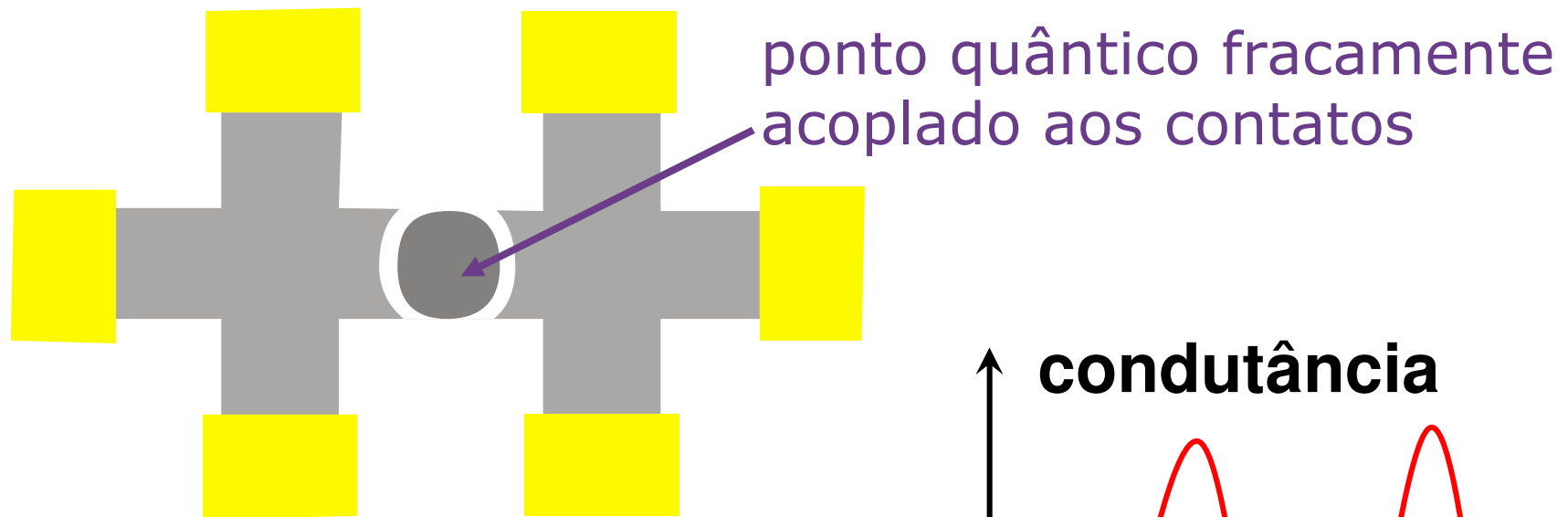
*$\sim 200.000 \text{ cm}^2/\text{V.s}$ a $4K$
(grupos de Kim e Andrei)*

*Grafeno suspenso
Intrínseco (limitados por fonons)
 $> 200.000 \text{ cm}^2/\text{V.s}$ a $300K$
(maior que qualquer outro
material conhecido)*

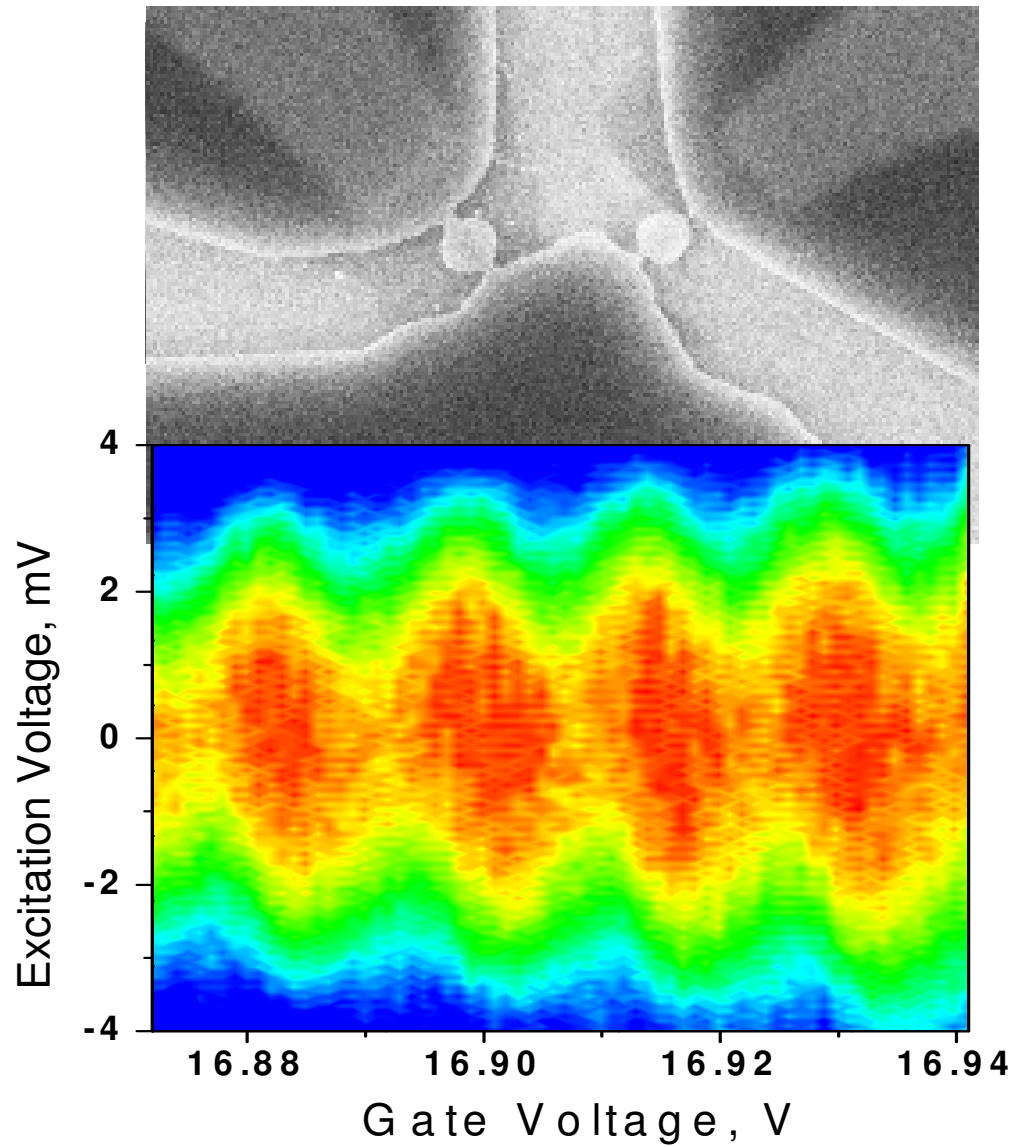
Transporte quase-balístico a condições ambientes?

Qualidade cristalina: poucos defeitos (1 por μm^2)

Ponto quântico de grafeno

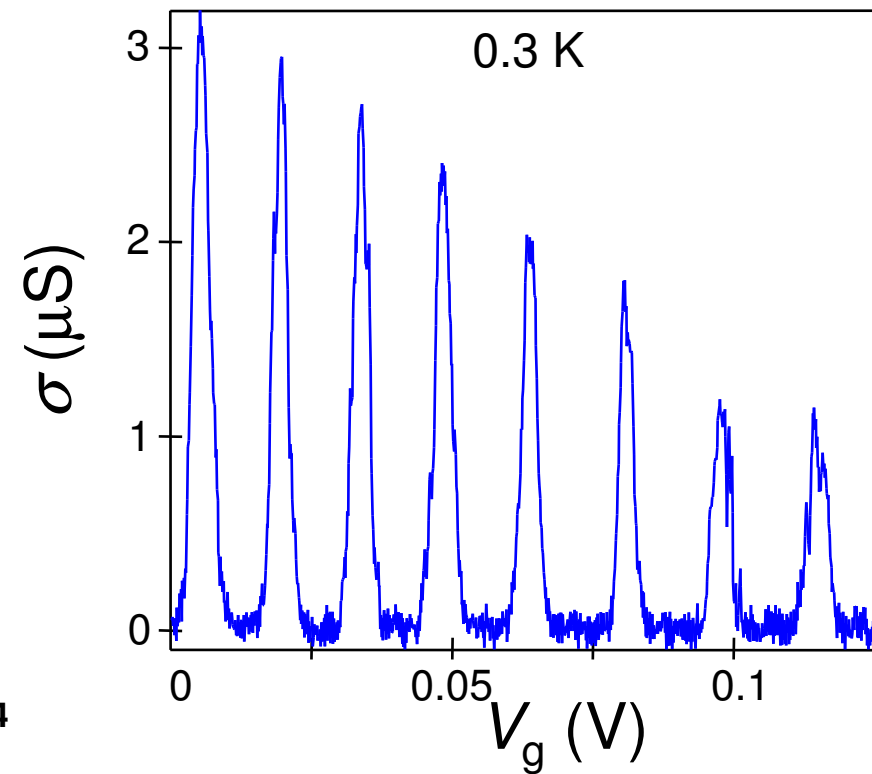


Ponto quântico de grafeno

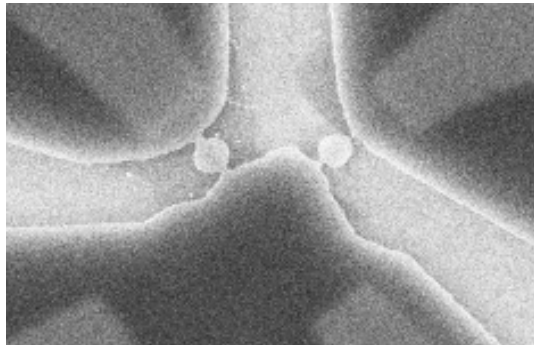


Transistor de um
único elétron

Geim *et al*,
Nature Materials 2007

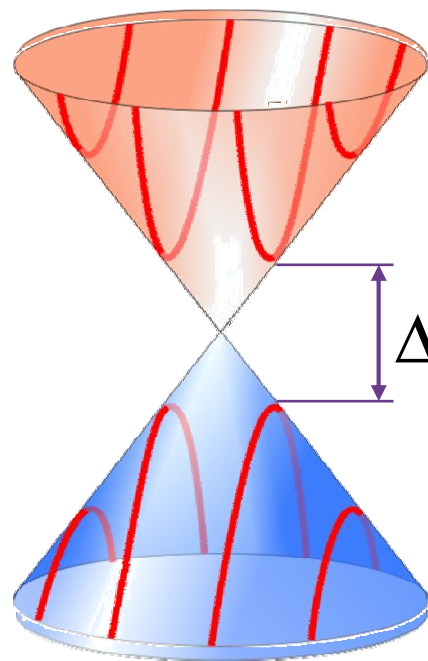


Ponto quântico de grafeno

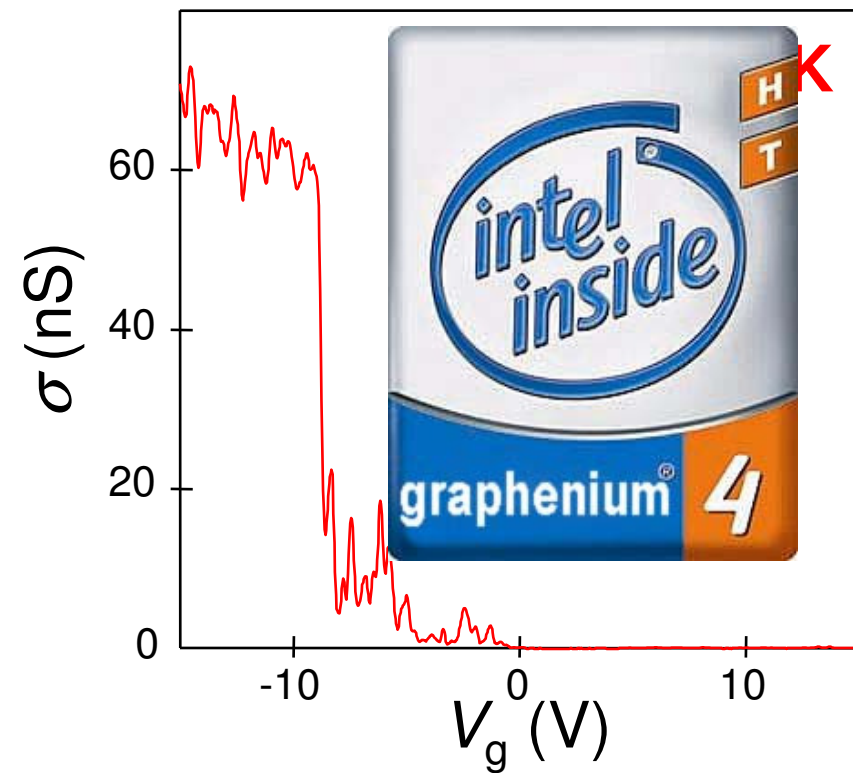


Temperatura ambiente
Transistor de um único elétron

Geim *et al*,
Nature Materials 2007



$$\Delta E = \frac{25.000 K}{L[nm]}$$

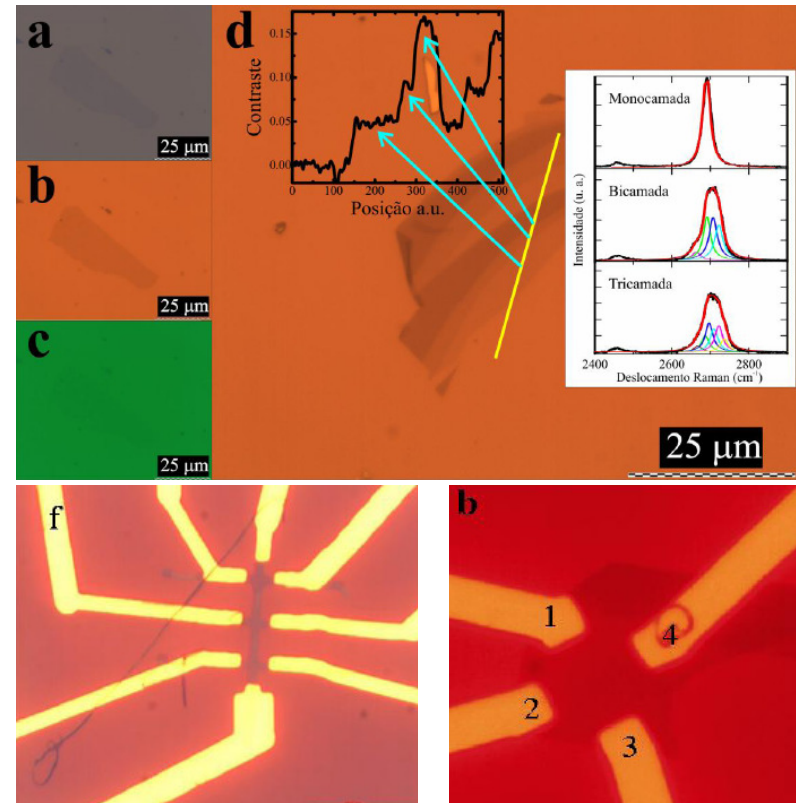


Grafeno no Brasil

- Grupo da UFMG e colaboradores
- Grupo da USP-SP: transporte eletrônico
- Grupo da Unicamp: compostos grafíticos
- Grupos teóricos (UFRJ,UFF,USP, entre outros)

INCT de Materiais de Carbono

- Síntese:
 - esfoliação mecânica;
 - crescimento epitaxial;
 - síntese química;
 - processamento de amostras
- Caracterização:
 - espectroscopia Raman;
 - microscopia eletrônica;
 - técnicas de luz síncrotron;
 - microscopia de tunelamento
- Modelagem:
 - teoria do funcional da densidade



Cortesia D. Elias

O nascimento do grafeno... e muito mais por vir....

